IMPROVING VOLTAGE SAG AND VOLTAGE SWELL OF DISTRIBUTION SYSTEM WITH INTEGRATION OF ULTRA CAPACITOR AND DYNAMIC VOLTAGE RESTORER

MSC THESIS

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BY

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LIST OF ABBREVIATION

APF	Active power filter
BESS	Battery energy storage system
C	Capacitance
DC	Direct current
DLG	Double line to ground
DSC	Distribution series capacitors
DSTATCOM	Distribution static synchronous compensators
DVR	Dynamic voltage restorer
EEP	Ethiopian Electric Power
EEU	Ethiopian Electric Utility
ep	Proportional error
EPR	Equivalent parallel resistor
ESR	Equivalent series resistor
FACTS	Flexible AC transmission system
GTO	Gate turns of thyristors
IEC	International Electro technical Commission
IEEE	Institute of electrical and electronics engineers
IGBT	Integrated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
Ki	Integral gain factor
Kp	Proportional gain
LL	Line to line
MOSFET	Metal oxide semiconductor field effect transistor
PCC	Point of common coupling
PI	Proportional integration
PI	Proportional integral
PLL	Phase locked loop
PQ	Power quality
PWM	Pulse width modulation
R	Resistance

S	Bypass switch
SA	Surge arrestors
SEMI	Semiconductor equipment and material international
SETC	Static electronic tap changers
SLG	Single line to ground
SMESS	Supper conducting magnetic energy storage system
SSFCL	Solid state fault current limiter
SSTS	Solid-state transfer switch
SVC	Static Var compensator
Ti	Integral time
TSC	Thyristor switched capacitor
UCAP	Ultra capacitor
UPFC	Unified power flow controller
UPS	Uninterrupted power supply
VDVR	Voltage of DVR
VL	Load voltage
Vref	Reference voltage
VSC	Voltage source converter
VSI	Voltage source inverter

ABSTRACT

Power Quality (PQ) problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure of end use equipments. The supply status of electrical services required for case study of Agro Processing Industry illustrates this concept. The voltage sag and swell are the most frequent PQ problems that mainly occur in the distribution systems because of it causes circuit breaker tripping, failure of drive systems, shutdown for domestic and industrial equipment. The Dynamic Voltage Restorer (DVR) connected in series has magnificent dynamic capabilities and is a flexible solution for PQ problems. Ultra-Capacitors (UCAP) has ideal characteristics such as high power and low energy density essential for the mitigation of voltage sag and swell. In this proposed research voltage sag and voltage swell problem are improved by using the method of integration of Ultra Capacitor and Dynamic Voltage Restorer device. In this study UCAP was used as energy storage as it provides excessive power in a short time interval of time. Integrated DVR into Ultra Capacitor via bidirectional DC-DC converter which supports in presenting a rigid dc-link voltage and helps in compensating temporary voltage sag and voltage swell. The integrated UCAP-DVR is implemented at low voltage side of distribution transformer. PI Controller was used in DVR for power quality enhancement. The simulation results carried out by Matlab/Simulink verify the performance of the proposed method. In the proposed system the voltage sag is mitigated from 0.304 p.u to 1p.u and the voltage swell is compensated from 1.125p.u to 1p.u.

Key word: Dynamic Voltage Restorer (DVR), Ultra-capacitor (UCAP), DC-DC converter, sag, swell, power quality, PI controller, MATLAB.

1. INTRODUCTION

1.1 Background

Power quality problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure of end use equipments. In recent years the concept of PQ in utility side has gotten dire attention. Due to the continuous growth of electric load and transfer of high regional power via a large interconnected network, the security of power system may reduce and leads to a complex operation. It creates with a broad range of disturbances such as harmonics, voltage sags, voltage swells, flicker, interruptions and other distortions [1, 2]. Among these power quality problems voltage sag and swell are the most frequent problems in the distribution system. Voltage sag occurs when the supply voltage drops with amplitude varies from 10% to 90% and lasts for a time duration of half a cycle to one minute [3]. Alternatively, Voltage swell may occur when the sudden rise of supply voltage with amplitude ranges from 110% to 180% of its nominal value [3]. A typical duration of voltage sag and swell is 10 ms to 1 minute according to IEEE 1159-1195 and IEEE 519-1992 standards. The mitigation can be done with a number of available methods using custom power devices such as DSTATCOM, DVR and UPFC. Among the custom power devices, Dynamic Voltage Restorer (DVR) is used as the most efficient device to restore the quality of voltage [4]. The voltage capability of DVR depends on the ability of maximum voltage injection.

Ultra-capacitors have various potential advantages that make them unbeatable in many applications because they require neither cooling nor heating, no moving parts, it does not undergo internal chemical changes as part of their function. In addition, no frequent maintenance is required with reduction in lifetime, degradation due to deep cycling and they are very efficient and robust.

A Dynamic Voltage Restorer (DVR) is power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages. The integration of UCAP based DVR is required. While DVR can supply only limited amount of real power and is not able to compensate for higher values of PQ problems. The UCAP-DVR connected via bidirectional DC-DC converter implemented. It is used to achieve a precise and fast response of the DVR. In addition, UCAPs have high power density and low energy density ideal characteristics for effective compensation of PQ problems such as voltage sag and voltage swell investigating the high quality of power in the distributed power generation.

1.2 Statement of the Problem

The necessity of designing the integration of ultra capacitor (UCAP) and dynamic voltage restorer (DVR) is by standing from the challenge of power quality problem. Due to the continuous growth of electric load and transfer of high regional power through a large interconnected network, the quality of power system may reduce and leads to a complex operation. So Hawassa substation distributes power with two 15KV transformers at the same terminal bus bar and also the distributor transformers are taped at the same terminal bus bar for each of feeders. Therefore, during a large load /motor starts at neighboring site the voltage reduction will occur at the nearest distribution and also when the distributor become with sudden rise of voltage supply, it causes increased voltage at the nearest distributor transformer. Depend on the duration of the interruption these increased and reduced voltage are results in voltage swell and voltage sag respectively.

However the general causes of power supply interruption at Hawassa distribution system is categorized in terms of temporary short circuit, temporary earth fault, permanent short circuit, permanent earth fault and system over load. This disturbance and fluctuation of voltage causes the circuit breaker tripping, product waste, system interruption and etc.

Voltage sags are one of the most dominating power quality assets, which dragged the attention of many researchers as the sensitivity of loads are increasing due to extensive usage of power electronic devices.

1.3 Objective of Research

1.3.1 General Objective

The objective of this study is to improve the voltage sag and voltage swell of Agro processing Industry power distribution with the integration of ultra capacitor and dynamic voltage restorer (UCAP-DVR).

1.3.2 Specific objective

- To reduce voltage sag and voltage swell.
- To implement UCAP-DVR for load voltage compensation.
- Sizing of UCAP-DVR according to specified load.
- To use MATLAB/Simulink for the result interpretation.
- Finally, to compare the results according to specified standard (IEEE 1159:1995).

2. LITERATURE REVIEW

There have been numerous implementations of several Flexible AC Transmission Systems (FACTS) devices controller for various applications worldwide. A number of new types of devices are in the stage of being introduced practically. Some of the devices include: Active Power Filters (APF), Battery Energy Storage Systems (BESS), Distribution Static synchronous Compensators (DSTATCOM), Distribution Series Capacitors (DSC), Dynamic Voltage Restorer (DVR), Surge Arresters (SA), Super conducting Magnetic Energy Systems (SMES), Static Electronic Tap Changers (SETC), Solid-State Transfer Switches (SSTS), Solid State Fault Current Limiter (SSFCL), Static Var Compensator (SVC), Thyristor Switched Capacitors (TSC) and Uninterruptible Power Supplies (UPS). The most research was done with related to these devices, though there can be the best solution and efficient if we integrate the Ultra capacitor with Dynamic voltage restorer to improve the power quality problem [5].

Few of the research related to integrated ultra capacitor and Dynamic Voltage Restorer (DVR) are listed below.

G. RAMESWARA REDDY, Assistant Professor, KBR Engineering College, Nalgonda, India done research for “ improving Power Quality of Distribution Grid with Ultra capacitor Integrated Power Conditioner” in 2015.

On his paper UCAP integration gives the power conditioner active power capability, which is useful in tackling the grid intermittencies and in improving the voltage sag and swell compensation. UCAPs have low energy density, high-power density and fast charge/discharge rates, which are all ideal characteristics for meeting high-power low-energy events like grid intermittencies sags/swells [6].

Chellali Benachaiba, Brahim FERDI Bechar University Center, Algeria researched on “Voltage Quality Improvement Using DVR” in 2008. He proposed the Dynamic Voltage Restorer (DVR), which is the most efficient and effective modern custom power device used in power distribution networks. Its appeal includes lower cost, smaller size, and its fast dynamic response to the disturbance [2].

Gajanan .M. Dhole Electrical Engineering Department, R. H. Sapat College of Engineering, Management Studies and Research, Nasik, India researched on “Sag and Unbalance Mitigation using DVR in Three-phase Four-wire Distribution Network” in 2016.

He proposes a control strategy for Dynamic Voltage Restorer to correct voltage sag as well as to mitigate the zero-sequence components in distribution system [7].

Aziz Tashackori faculty of electrical and computer engineering university of Tapriz, Iran researched on “power quality improvement using a power electronics transformer based DVR” in 2015. In his paper a three phase four wire dynamic voltage restorer (DVR) with bidirectional power electronics transformer structure is proposed to inject required compensating series voltage to the electric power system [8].

S. Sellakumar Associate Professor Department of Electrical and Electronics Engineering Jeppiaar Engineering College, Chennai India done the research on the “ Cascaded Inverter Based Hybrid Shunt Active Filter to Improve the Power Quality of 415V 50Hz four wire Distribution Systems” **i**n 2014. He proposed that the Shunt AF filters can be used in multilevel mode to enhance the power quality. Cascaded multilevel Inverter is used as Shunt Active Power Filter to compensate the voltage sag during the presence of non-linear loads with reduced harmonics [9].

G.v.r satyanarayana EEE department, v.r.siddhartha engineering college, Vijayawada, India is done the research on “cascaded 5-level inverter type DSTATCOM for power quality improvement” in 2010. This study proposes a cascaded multilevel inverter type DSTATCOM to compensate voltage sags in utility voltages in power distribution network. The proposed DSTATCOM is implemented using multilevel topology with isolated dc energy storage [9].

2.1 Electric Power Quality Problem

The main concern of consumers of electricity is the reliability of supply. Even though the power generation in most advanced countries is fairly reliable, the distribution is not always so. Now a day’s consumers want not only reliability also quality of power system is very important to them. For example, a consumer that is connected to the same bus that supplies a large motor load may have to face a severe dip in his supply voltage every time, when the motor load is switched on. In some extreme cases, it may have to stand with blackout.

There are also very sensitive loads such as hospitals (life support, operation theatre and patient database system), processing plants (semiconductor, food, rayon and fabrics), air traffic control, financial institutions and numerous other data processing and service providers that require clean and uninterrupted power [10].

In several processes such as semiconductor manufacturing or food processing plants, a batch of product can be ruined by a voltage dip of very short duration. Such customers are very wary of such dips since each such interruption cost them a substantial amount of money. Even short dips are sufficient to cause contactors on motor drives to drop out. Stoppage in a portion of a process can destroy the conditions for quality control of the product and require restarting of production. Transmission lines are exposed to the forces of nature. Furthermore, each transmission line has its load ability limit that is often determined by either stability considerations or by thermal limits. Even though the power quality problem is a distribution side problem and transmission lines often have an impact on the quality of power supplied. It is however to be noted that while most problems associated with transmission systems arise due to the forces of nature or due to the interconnection of power systems, individual customers are responsible for a more substantial fraction of the problems of power distribution systems [10].

2.2 Sources and effects of power quality problems

Power distribution systems ideally, should provide their customers with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency. However, in practice power systems, especially the distributions have numerous nonlinear loads, which significantly affect the quality of power supplies. As a result of the nonlinear loads, the purity of the waveform of supplies is lost. This ends up producing many power quality problems.

While power disturbances occur on all electrical systems, the sensitivity of today’s sophisticated electronic devices makes them more susceptible to the quality of power supply. For some sensitive devices, a momentary disturbance can cause scrambled data, interrupted communications, a frozen mouse, system crashes and equipment failure etc. A power voltage spike can damage valuable components. Power Quality problems encompass a wide range of disturbances such as voltage sags, swells, flicker, harmonics distortion, impulse transient and interruptions [10].

i. **Sag (Dip):** is a decrease between 0.1p.u and 0.9p.u in R.M.S. Voltage or current at the power frequency for durations from 0.5 cycles to 1 min [11].
ii. **Swell:** is an increase between 1.1p.u and 1.8 p.u of R.M.S voltage or current at the power frequency for durations from 0.5 cycles to 1 min [11].

iii. **Harmonics:** are sinusoidal voltages or currents having frequencies that are integer multiplies of the frequency at which the supply system is designed to operate. Harmonic distortion originates in the non-linear characteristics of devices and loads on the power system.

iv. **Interruption:** occurs when the supply voltage or load current decreases to less than 0.1 Pu for a period of time not exceeding 1 min [11]. These are the results of faults, equipment failures and control malfunctions.

v. **Impulsive transient** is a sudden, non-power frequency change in the steady state condition of voltage, current, or both that is unidirectional in polarity [12].

2.2.1 Causes of voltage sags

Voltage sag are experienced when other customers share a common supply impedance with an over current event on the supply system or in customer premises. Since Hawassa substation distributes power system with two 15kv transformer and 33kv transformer for the city. These transformers totally have 14 feeders. Ten feeders are connected with 15KV at point of common coupling (PCC) or at the same terminal bus. Figure 2.1 drawn by ProfiCAD software shows for a fault clearing or switching at point A of the incoming feeder or fault in the distribution feeder-I, the voltage at feeder-2 will sag. Without the presence of the custom device, this will trip the sensitive load causing a loss of production. At the low voltage supply a frequent cause of complaint is dips caused by motor starts in neighboring premises. The severity of the dip is high when a low voltage transformer is rated to supply a very few customers. A higher rating transformer feeding a larger number of customers reduces the depth of the voltage dip but affects more customers. A fault on a higher voltage supply to customers such as l5kV connection can affect a much larger number of customers. The general causes of voltage sag are [13]:

1. Rural location remote from power source
2. Unbalanced load on a three phase system
3. Switching of heavy loads
4. Long distance from a distribution transformer with interposed loads
5. Unreliable grid systems
6. Equipments not suitable for local supply
7. Short circuit and motor starting

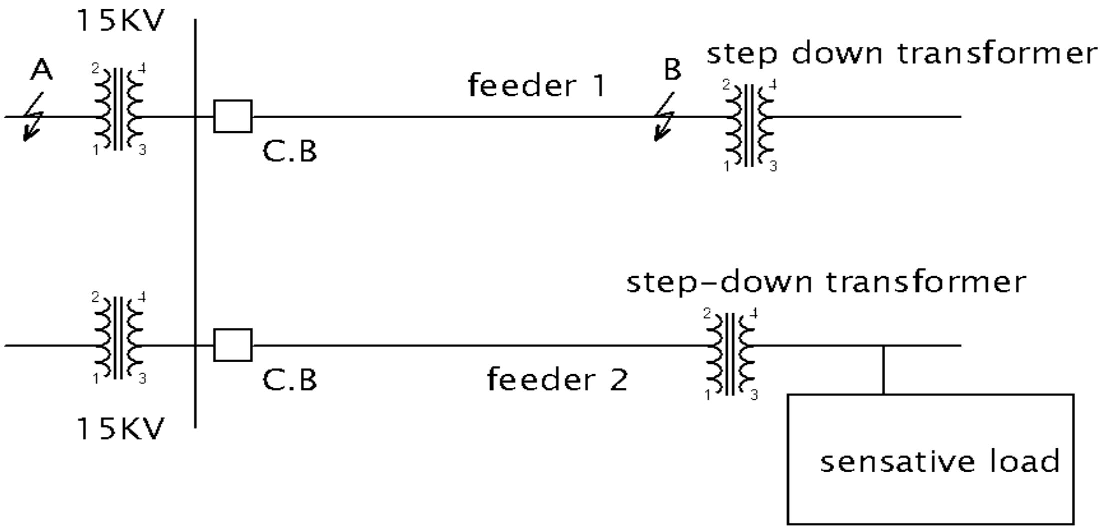

Figure 2.1: sources of voltage disturbance

2.2.2 Voltage sag calculation

The basics voltage sags that take place by the three elementary types of short circuit are usually required in fault studies that are the Single line to ground fault (SLG), Line to Line fault (LL) and Double Line to Ground fault (DLG) [14] .

Voltage sags are usually caused by short –circuit current into fault and a simplified model is illustrated in fig 2.2. Magnitude and phase of the voltage sag at the point of common coupling (PCC) are determined by the fault and supply impedances, using the following equation [15]:

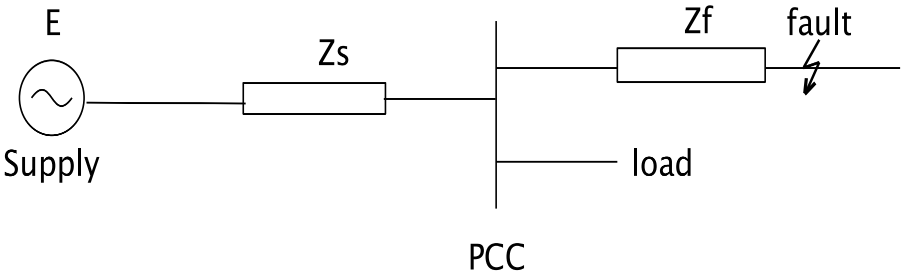

Figure 2.2: Simplified circuit for voltage sag calculation

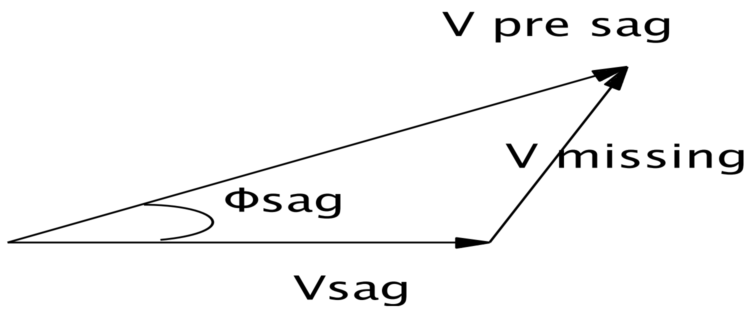

Figure 2.3: Vector diagrams of various voltages during sag

$$\text{Vsag} = E\,\frac{Zfault}{Zfault+Zsupply} \tag{2.5}$$

By the impedance considerations the reduced magnitude and in some cases a phase jump can be estimated. Figure 2.7 illustrates the used definitions of the voltage at the PCC with Vsag as the voltage during the sag and Φsag is the phase jump at PCC. Simple symmetrical voltage sag can be characterized by the following three parameters.

- Voltage during sag (Vsag)
- Sag duration (tsag)
- Phase jump (Φsag)

The definition of voltage sag with phasors can be stated as:

Vsag = V presage – V missing

As per the definition, the voltage sag is the voltage at PCC during the voltage sag and can be calculated as pre-sag voltage (often the rated voltage) subtracted the missing voltage. In order to have full compensating, the DVR must inject the missing voltage. If the voltage sag is severe, Vsag is low and shallow voltage sag is characterized as high Vsag value.

2.2.3 Causes of voltage swell

Voltage swell are usually associated with system fault condition just like voltage sag but are much less common. This is particularly true for ungrounded or floating delta systems, where the sudden change in ground reference result in a voltage rise on the ungrounded phase. In the cases of a voltage swell due to a single line-to- ground (SLG) fault on the system, the result is a temporary voltage rise on the unfaulted phases, which last for the duration of the fault.

Voltage swell can also be caused by the de-energization of a very large load, start – stop of heavy loads, poor system voltage regulation and bad dimensioned power supply and bad regulated transformer mainly at off-peak hours [16]. The abrupt interruption of current can generate a large voltage per the formula:

$V = L\, di/dt$

Where L - is the inductance of the line and

Di/dt – is the change in current flow.

More ever the energization of large capacitor bank can also causes a voltage swell, though it more causes an oscillatory transient. The effect of voltage swell may cause break down of components on the power supply of the equipment, though the effect may be a gradual accumulative effect. It can cause control problems and hardware failure in the equipment, due to overheating that could eventually result to shut down. Also electronics and other sensitive equipment are become to damage due to voltage swell.

Voltage swell is defined by IEEE 1159 as the increase in the RMS voltage level from 110% to 180% of nominal, at the power frequency for durations of half cycle to one minute. According to IEEE 1159 standards voltage swell are subdivided into three categories. They are instantaneous, momentary and temporary which is shown in table 3.2 in next section with their magnitude and duration.

2.2.4 Monitoring and Mitigation of power quality problem

Power quality variations are classified as either disturbances or steady state variations. Disturbances affect to abnormalities in the system voltages or currents due to fault or some abnormal operations. Steady state variations refer to rms deviations from the nominal quantities or harmonics [12].

In general these are monitored by disturbance analyzers, voltage recorders, harmonic analyzers etc. However with the advancement in the computer technology, better, faster and more accurate instruments can now be designed for power quality monitoring and analysis.

The input data for any power quality monitoring device is obtained through transducers. These include current transformers, voltage transformers, Hall-effect current and voltage transducers etc. Disturbance analyzers and disturbance monitors are instruments that are specifically designed for power quality measurements.

There are two approaches to mitigate power quality problems. First approach is called load conditioning, which ensures that the equipment is less sensitive to power disturbances, allowing the operation even under significant voltage distortion. The other solution is to install line conditioning systems that suppress or counteracts the power system disturbances. The solution to the power quality can be done from customer side or from utility side. The custom device systems or utility side solutions will play a major role in improving the inherent supply quality. Some of the effective and economic measures can be identified as follows.

I. Surge Arresters

Arresters are designed for lightening protection of transformers, but are not sufficiently voltage limiting for protecting sensitive electronic control circuits from voltage surges.

II. Energy Storage Systems

Storage systems can be used to protect sensitive production equipments from shutdowns caused by voltage sags or momentary interruptions. These are usually DC storage systems such as UPS, batteries, superconducting magnet energy storage (SMES), storage capacitors or even fly wheels driving DC generators .The output of these devices can be supplied to the system through an inverter on a momentary basis by a fast acting electronic switch. Enough energy is fed to the system to compensate for the energy that would be lost by the voltage sag or interruption.

Though there are many different methods to mitigate voltage sags and swells, but the use of a custom Power device is considered to be the most efficient method. Some of the custom power device listed below.

III. Static Var Compensator (SVC)

There are two main building blocks for SVCs - thyristor switched capacitor and thyristor controlled reactor. In a thyristor switched capacitor (TSC), a capacitor is connected in series with two opposite poled thyristors [10]. In a thyristor controlled reactor (TCR), a reactor is connected in series with two opposite poled thyristors. One of these thyristors conducts in each positive half cycle of the supply frequency, while the other conducts in the corresponding negative half cycle.

IV. Thyristor Controlled Series Compensator (TCSC)

The TCSC contains an ac capacitor that is connected in parallel with a TCR. This is a series compensation device, its placement is not that crucial and it can be placed anywhere along the line.

V. Static Compensator (STATCOM)

This is a shunt device that does not require passive elements like inductors and capacitors. The STATCOM is built around a voltage source inverter, which is supplied by a dc capacitor. The inverter consists of GTO switches which are turned on and off through a gate drive circuit. The output of the voltage source inverter is connected to that ac system through a coupling transformer.

VI. Unified Power Flow Controller (UPFC)

UPFC contains two voltage source inverters that are connected together through a dc link capacitor. The three ways of operating the UPFC are, as a shunt controller, as a series controller and also as phase angle regulator.

VII. Distribution STATCOM (DSTATCOM)

This is a shunt connected device which perform load compensation, i.e., power factor correction, harmonic filtering, load balancing etc. when connected at the load terminals. It can also perform voltage regulation when connected to a distribution bus.

3 MATERIALS AND METHOD

3.1 Materials

3.1.1 Dynamic Voltage Restorer

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer (DVR). This device employs IGBT solid-state power-electronic switches in a pulse-width modulated (PWM) inverter structure [10]. The DVR is capable of generating or absorbing independently controllable real and reactive power at its ac output terminal. The DVR is made of a solid-state dc to ac switching power converter that injects a set of three-phase ac output voltages in series and synchronism with the distribution feeder voltages. The amplitude and phase angle of the injected voltages are variable thereby allowing control of the real and reactive power exchange between the DVR and the distribution system. The dc input terminal of a DVR is connected to an energy source or an energy storage device of appropriate capacity. The reactive power exchanged between the DVR and the distribution system is internally generated by the DVR without ac passive reactive components. The real power exchanged at the DVR output ac terminals is provided by the DVR input dc terminal by an external energy source or energy storage system.

A typical DVR connection is shown in Figure 3.l below. It is connected in series with the distribution line that supplies a sensitive load. Without the presence of the DVR, this will trip the sensitive load causing a loss of production. The DVR can protect the sensitive load by inserting voltages of controllable amplitude, phase angle and frequency (fundamental and harmonic) into the distribution feeder via a series insertion transformer as shown in Figure 3.1. DVR can only supply partial power to the load during very large variations (sags or swells) in the source voltage.

The two different structures of the DVR are shown in Figure 3.1 [8]. In the structure of Figure 3.1 (a), the dc bus of the VSI realizing the DVR is supplied from the feeder through a rectifier. Therefore the DVR can absorb real power from the feeder through the dc bus. This is not possible for the structure of Figure 3.1 (b) in which the DVR is supplied by a dc storage capacitor.

Therefore the DVR in this structure must operate in the mode in which it will have no real power exchange with the ac system in the steady state. In this study the VSI realizing of the DVR is supplied from the feeder through a rectifier is implemented.

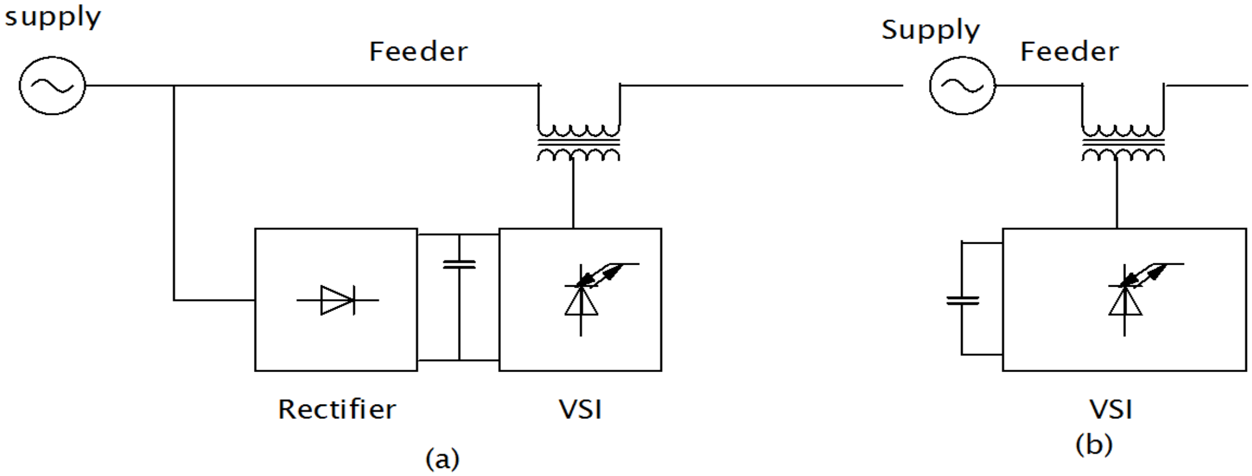

Figure 3.1: Different structures of DVR [18]

3.1.2 DVR Structure

In DVR structure the voltage sources are realized by voltage source inverters (VSI).There are capacitor filter and inductor – capacitor filter realization.

In capacitor case the three VSIs are connected to a common dc storage capacitor. In this case each switch represents a power semiconductor device and an anti-parallel diode combination. Each VSI is connected to the network though a transformer and a capacitor filter. The transformers not only reduce the voltage requirement of the inverters but also provide isolation between the inverters. This prevents the dc storage capacitor from being shorted through switches in different inverters. In the DVR structure of the capacitor filter is connected across the secondary of the transformer. This prevents switching frequency harmonics from entering the system. The main drawback of the system is that the direct connection of VSI to the transformer primary results in losses in the transformer [10]. The high frequency flux variation causes significant increase in transformer iron losses. To avoid this, a switch frequency LC filter (LCf) is placed in the transformer primary as shown in Figure 3.2 below. The secondary of the transformer is directly connected to the feeder. This will limit the switch frequency harmonics too mainly in the primary side of the transformer. The DVR structure and it location at customer side diagram is drawn by ProfiCAD software is shown in figure 3.2 below.

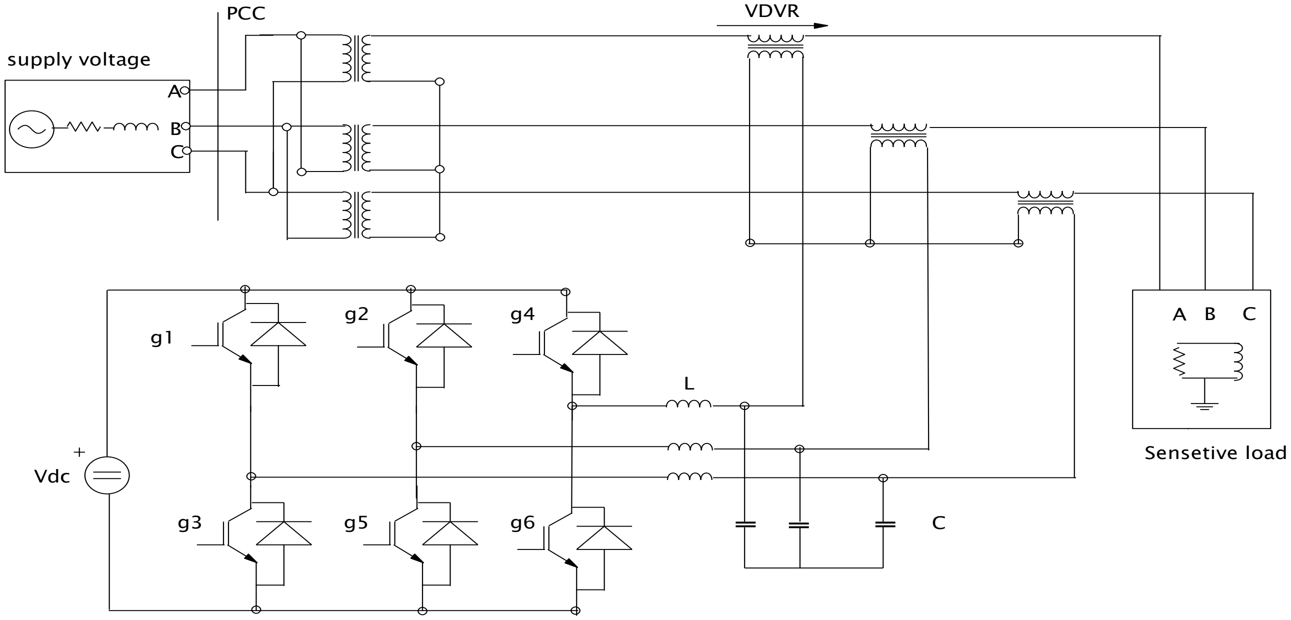

Figure 3.2: DVR structure and its location [10]

3.1.3 The basic components of a DVR

DVR can be applied for medium voltage and in low voltage application [17]. Figure 3.2 above shows conventional circuit configuration of the DVR. DVR basically consists of the [3, 4,5,10 and 17] following parts:

I) Series Voltage Injection/booster Transformers

The injection/booster transformer limits coupling or mixture of noise and transient energy from primary to secondary side [18]. Generally High voltage side of the injection transformer is connected in series to the distribution system and the power circuit of the DVR can be connected at the low voltage side. Its main function are: connects DVR to the distribution system through HV-winding and transforms and couples the injected compensating voltages generated by VSC to incoming supply voltage, to increase the voltage supplied by the filtered VSI output to the desired level while isolating the load from the system (VSC and control mechanism).The transformer winding ratio is pre-determined according to the voltage required at the secondary side of the transformer basically it is kept equal to supply voltage to allow DVR to compensate for full voltage sag. A higher transformer winding ratio will increase the primary side current, which will adversely affect the performance of the power electronic devices connected in the VSI [18].

II. Voltage Source Inverter (VSI)

A VSC is power electronic system consists of a storage device and switching devices. It generates a sinusoidal voltage at any required frequency, magnitude and phase angle. The function of an inverter system in DVR is used to convert the DC voltage supplied by the energy storage device into an AC voltage [17] and to temporarily replace the supply voltage or to generate part of supply voltage which is missing. Numerous circuit topologies are available for the VSC [12, 18]. A widely used method is the two level or multilevel three-phase converters which shares a dc capacitor between all phases. The purpose of this capacitor is mainly to absorb harmonic ripple and hence it has a relatively small energy storage requirement, particularly when operating in balanced conditions. The size of this capacitor has to be increased if needed to provide voltage support in unbalanced conditions.

Also, as the capacitor is shared between the three phases, sag on only one phase may cause a distortion in the injected current waveforms on the other phases. Another popularly used converter topology is the H-bridge cascade inverter [3]. Converters with this topology are suitable in high voltage and power system applications due to their ability to synthesize waveforms with better harmonic spectrums, and attain higher voltages with a limited maximum device rating.

III. Switching Devices

There are four main types of switching devices: Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Gate Turn-Off thyristors (GTO), Insulated Gate Bipolar Transistors (IGBT) and Integrated Gate Commutated Thyristors (IGCT). Each type has its own benefits and drawbacks. The MOSFET requires a high on-resistance and has fast switching times [18]. It is capable of working beyond the 20 kHz frequency [18]. The limitations are that the increasing on-resistance with increasing voltage limits the device to applications with just a few hundred volts.

The GTO is a latching device that can be turned off by a negative pulse of current to its gate [19]. The GTO is best suited for high voltage applications [20]. The disadvantages of the GTO are that GTO based devices are not able to meet the dynamic requirements of a DVR. The IGBT is considered to be a newer device compared to the MOSFET and GTO. In essence, it is a three terminal controllable switch that combines the fast switching times of the MOSFET with the high voltage capabilities of the GTO. The result of this combination is a medium speed controllable switch capable of supporting the medium power range.

The IGCT is a recent compact device with enhanced performance and reliability that allows building VSC with very large power ratings. Because of the highly sophisticated converter design with IGCTs, the DVR can compensate dips which are beyond the capability of the past DVRs using conventional devices.

IV. Passive Filters

In DVR, filters convert the inverted PWM waveform into a sinusoidal waveform, by eliminating the unwanted harmonic components generated by the VSI action.

Passive filters are inductance, capacitance and resistance elements configured and tuned to control harmonics. They are commonly used and are relatively inexpensive compared with other means for eliminating harmonic distortion. However, they have the disadvantage of potentially interacting adversely with the power system and it is important to check all possible system interactions when they are designed. They are employed either to shunt the harmonic currents off the line or to block their flow between parts of the system by tuning the elements to create a resonance at a selected frequency.

i) **Shunt passive filters.** The most common type of passive filter is the single- tuned “notch” filter. This is the most economical type and is frequently sufficient for the application. The notch filter is series-tuned to present low impedance to a particular harmonic current and is connected in shunt with the power system. Thus, harmonic currents are diverted from their normal flow path on the line through the filter. Notch filters can provide power factor correction in addition to harmonic suppression. In fact, power factor correction capacitors may be used to make notch filters.

ii) **Series passive filters.** Unlike a notch filter which is connected in shunt with the power system, a series passive filter is connected in series with the load. The inductance and capacitance are connected in parallel and are tuned to provide high impedance at a selected harmonic frequency. The high impedance then blocks the flow of harmonic currents at the tuned frequency only.

V. DC charging circuit:

The dc charging circuit has two main functions: The first is to charge the energy source after sag compensation event and second is to maintain dc link voltage at the nominal dc link voltage. To charge the dc-link various topologies are used such as an external power supply or by connecting the dc side of the DVR to the controlled or uncontrolled rectifier to maintain the dc voltage. The other side of the rectifier can be from a main power line or from an auxiliary feeder.

There a rise an increasing need for the systems with the competency of bidirectional transfer of energy between two dc buses, thus bidirectional dc-dc converters have recently received a lot of attention. It acts as an interface circuit in energy storage system for UCAP as a wide range of voltage varies during charging and discharging. Moreover in the voltage side, if an inverter is connected, there is a need for the UCAP to provide a stable DC voltage for the inverter circuit. Thus, DC-DC converter plays a major role in this system. The model of bidirectional DC-DC converter is shown in Figure 3.3 with UCAP as energy storage.

During Voltage sag event, the DC-DC converter should be able to withstand the power generated during the discharge mode. Depend on depth and duration of the voltage sag; the system decides the amount of active power support. Conversely, during voltage swell event the DC-DC converter may able to absorb the additional power from the system [18]. Thus bidirectional DC-DC converter acts in boost mode while discharging and, on the other hand, it acts as buck mode during charging.

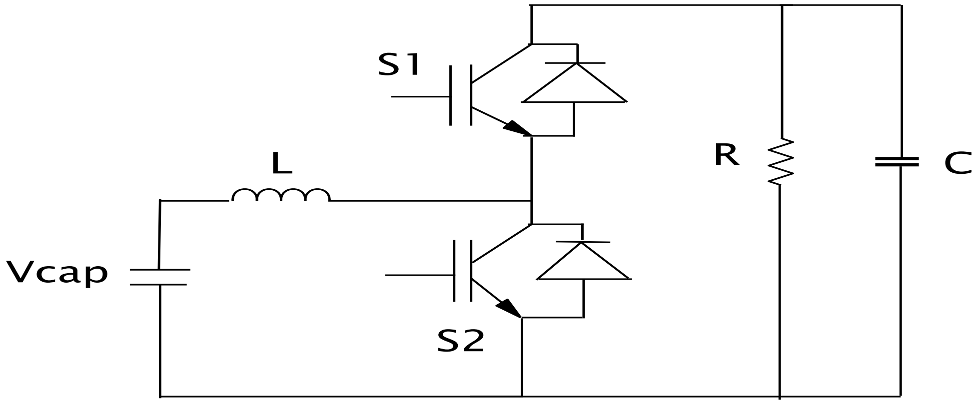

Figure 3.3: The model of Bidirectional DC-DC Converter with UCAP

A large number of DC-DC converter circuits are known that can increase or decrease the magnitude of the DC voltage or invert its polarity. In this proposed the switch is realized using a IGBTs semiconductor switches. The average output voltage (Vout) is a function of the duty cycle (D) of the IGBT switch.

In the buck converter, which reduces the dc voltage and has conversion ratio M (D) = D [14]. In a similar topology known as the boost converter, produces an output voltage (Vout) that is greater in magnitude than the input voltage (V_{in}). Its conversion ratio is M (D) = 1/ (1 – D).

In the buck-boost converter, the switch alternately connects the inductor across the power input and output voltages. This converter inverts the polarity of the voltage, and can either increase or decrease the voltage magnitude. The conversion ratio is M (D) = - D/ (1 – D).

Therefore the duty cycle (D) is decided from the requirement of the output voltage of the three level bridge IGBT switch and from the input voltage drop at dc-link.

$$\text{Vout} = \frac{1}{1-D} V_{in} \qquad (3.1)$$

3.1.4 Control system of the DVR output voltage

The control system of a DVR plays an important role, with the requirements of fast response in the face of voltage sags and variations in the connected load.

The main purpose of the control system is to maintain a constant voltage magnitude at the point where a sensitive load is connected, under system disturbances. It will also look after the D.C. link voltage using the DC-charging unit [12].

PI control is becoming more popular because of its ability to maintain exact set point. There are three main voltage controllers, which are Feed-forward (open loop), Feedback (closed loop) and Multi-loop controller [17]. The Feed-forward voltage controller is the primary choice for the DVR, because of its simplicity and fastness. The drawback of the open loop controller is the high steady state error. The Feedback controller has the advantage of accurate response, but it is complex and time-delayed. Multi-loop control is used with an outer voltage loop to control the DVR voltage and inner loop to control the load current.

3.1.5 Discrete pulse width modulation (PWM) -Based Control Scheme

The aim of discrete pulse modulation control scheme is to maintain a constant voltage magnitude at the sensitive load point, under the system disturbance [12].

The control system only measures the RMS voltage at load point, for example, no reactive power measurement is required.

The output pulses are a vector (with values= 0 or 1). Depending on the selected "Generator Mode", the output vector contains:

For a 1-arm bridge: Two pulses. Pulse 1 is for the upper switch and pulse 2 is for the lower switch.

For a 2-arm bridge: Four pulses. Pulses 1 and 3 are respectively for the upper switches of the first and second arm. Pulses 2 and 4 are for the lower switches.

For a 3-arm bridge: Six pulses. Pulses 1, 3 and 5 are respectively for the upper switches of the first, second and third arm. Pulses 2, 4 and 6 are for the lower switches.

For double 3-arm bridges: Twelve pulses. The first six pulses (pulses 1 to 6) must be sent to the first 3-arm bridge and the last six (pulses 7 to 12) to the second 3-arm bridge.

By selecting "Internal generation" we can control the modulation index m, frequency and phase of the output voltage from the internal parameters (m, Freq and Phase). Otherwise external signals are used for pulse generation. The width of the input vector must be 1 for single phase bridges (1-arm or 2-arm) and 3 for 3-phase bridges (single or double bridge).

3.1.6 Phase Sequence Analyzer

A Fourier analysis over a sliding window of one cycle of the specified frequency is first applied on the three input signals to find phasors V_a, V_b and V_c, at fundamental or harmonics frequency. Then, the Vabc to 120 transformations is applied to obtain the positive-sequence (V1), negative-sequence (V2) and zero-sequence (V0). We can use this block in a control system to measure a positive sequence voltage or current. It is not sensitive to harmonics or unbalances. However, as any filtered system, it introduces some delay. For example, its response to a step change of V1 is a one cycle ramp.

3.1.7 Ultra capacitors

Ultra capacitors are different from other capacitors types due to the electrodes used in these capacitors. Ultra capacitors are based on a carbon technology. The carbon technology used in these capacitors creates a very large surface area with an extremely small separation distance. Capacitors consist of 2 metal electrodes separated by a dielectric material.

The dielectric not only separates the electrodes but also has electrical properties that affect the performance of a capacitor. Ultra capacitors do not have a traditional dielectric material like ceramic, polymer films or aluminum oxide to separate the electrodes but instead have a physical barrier made from activated carbon that when an electrical charge is applied to the material a double electric field is generated which acts like a dielectric.

The capacitor is made up of a series of RC circuits where R1, R2 …Rn are the internal resistances and C1, C2..., Cn are the electrostatic capacitances of the activated carbons. When voltage is applied current flows through each of the RC circuits. The amount of time required to charge the capacitor is dependent on the C & R values of each RC circuit. Obviously the larger the C & R the longer it will take to charge the capacitor [22].

Ultra capacitor is double layer capacitor; the energy is stored by charge transfer at boundary between electrode and electrolyte. The amount of energy stored is the function of electrode surface, the size of ion and the level of electrolyte decomposition voltage. Ultra capacitor is constituted of separator and electrolyte electrode. The two electrodes are made up of activated carbon. On the electrode current collectors with a high conducting part assure the interface between the electrodes and the connection of ultra capacitor. The two electrodes are separated by membrane which allows the mobility of charged ions and prevent the electronic contact. The electrolyte supplies and conducts the ions from one electrode to other.

The parameters of ultra capacitor include capacitance (C), equivalent series resistance (ESR) and equivalent parallel resistance (EPR) is shown in figure 3.4.

Capacitance decides the energy storage capability of ultra capacitor. ESR is consists of electrode resistance, electrolyte resistance and contact resistance that wastes power for internal heating when charging or discharging of ultra capacitor. Also influences the energy efficiency and power density.

EPR is an inner equivalent parallel resistance that decide the leakage current when the ultra capacitor in standby mode.

To obtain the higher voltage and proper energy storage capacity, ultra capacitor is connected in series and parallel combination. The huge energy stored in ultra capacitor is unable to distribute to load due to its large equivalent series resistance; peak power is mainly limited by joule losses in the ESR of the ultra capacitor [18].

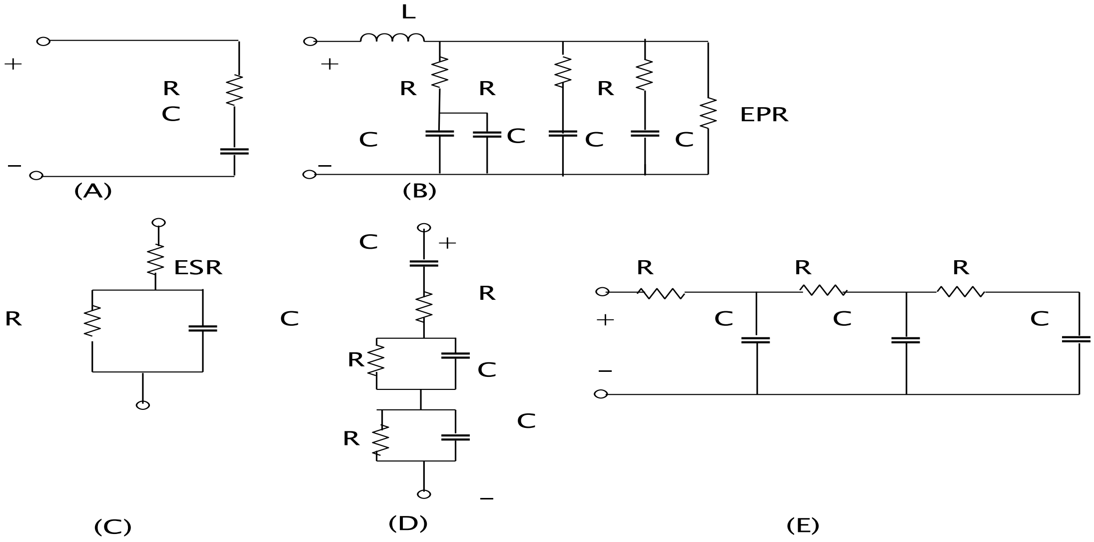

Figure 3.4: (A) Simple UC Model (B) RC parallel branch model (C) UC Model with ESR and Rp (D) RC Branch Series – Parallel Model (E) Transmission line model

Different authors are proposed the modeling of UCAP to study its electrical behavior under various operating condition. The model in Figure 3.4 (A), (C) and (D) are incomplete to describe the behavior of UC under various operating conditions. Therefore, more efficient ultra capacitors models have been proposed recently by many authors are shown in Figure 3.4 (B) and (E). In this study transmission line model of Ultra capacitor is selected to rate the size of Ultra capacitor according to specified load.

- **Ultra Capacitor function**

There is a lot of application of ultra capacitor.

- Secure power: provide reliable power even if the primary source fails or fluctuates.
- Energy storage: stores energy from low power source enabling support for high power loads.
- Pulse power: supplies peak power to the load while drawing average power from the source.
- User benefit: reduce the size and weight of the battery for power source required.
  - Improve run time and battery life (over 20 years), particularly at cold temperature [22].
  - Protect against accidental power loss or fluctuation/interruption.
  - Doesn't need to be replaced like battery (unlimited discharge cycle).
  - Environmentally friendly and safe.

Since the ultra capacitor is become to end life and failure mode during the phenomenon of over voltage, over temperature and mechanical stress.

3.2 Methodology

Improving the power quality of the system by integration of ultra capacitor and dynamic voltage restorer is involves the step of procedure. First it starts the collection of voltage disturbance data from the EEP, EEU, according to IEEE standard and interruption frequency from Hawassa substation. At Hawassa substation there are fourteen feeders. Then for each of feeder the power supply, current and the rated three phase voltage are identified. Depend on the amount of the voltage the integration of UCAP and DVR was designed by sizing all the equipment and component which is utilizes in this system depend on the load. During the fault the result of voltage sag and voltage swell without integration of UCAP –DVR and with UCAP –DVR connection in series to the line is shown by matlab/simulink modeling.

3.2.1 Data Analysis

In order to solve the voltage Sag and voltage Swell for distribution system the quantitative research methodology was used. This type of research methodology is used to rate the capacity of ultra capacitor storage, DC-DC converter, series inverter (DVR) in terms of voltage, current and power based on the load profile at the location.

The activities of this study will be classified into two steps:

First step: Review, Data collection and Analysis:

- Data was collected from EEP, EEU, general literature, website, international journals, different books, You Tubes and online information.

Second step: result and simulation was specified.

Based on the load requirement and specified the ultra capacitor, DC-DC convertor and DVR are rated. The simulation model for the proposing system is developed in MATLAB/simulink software.

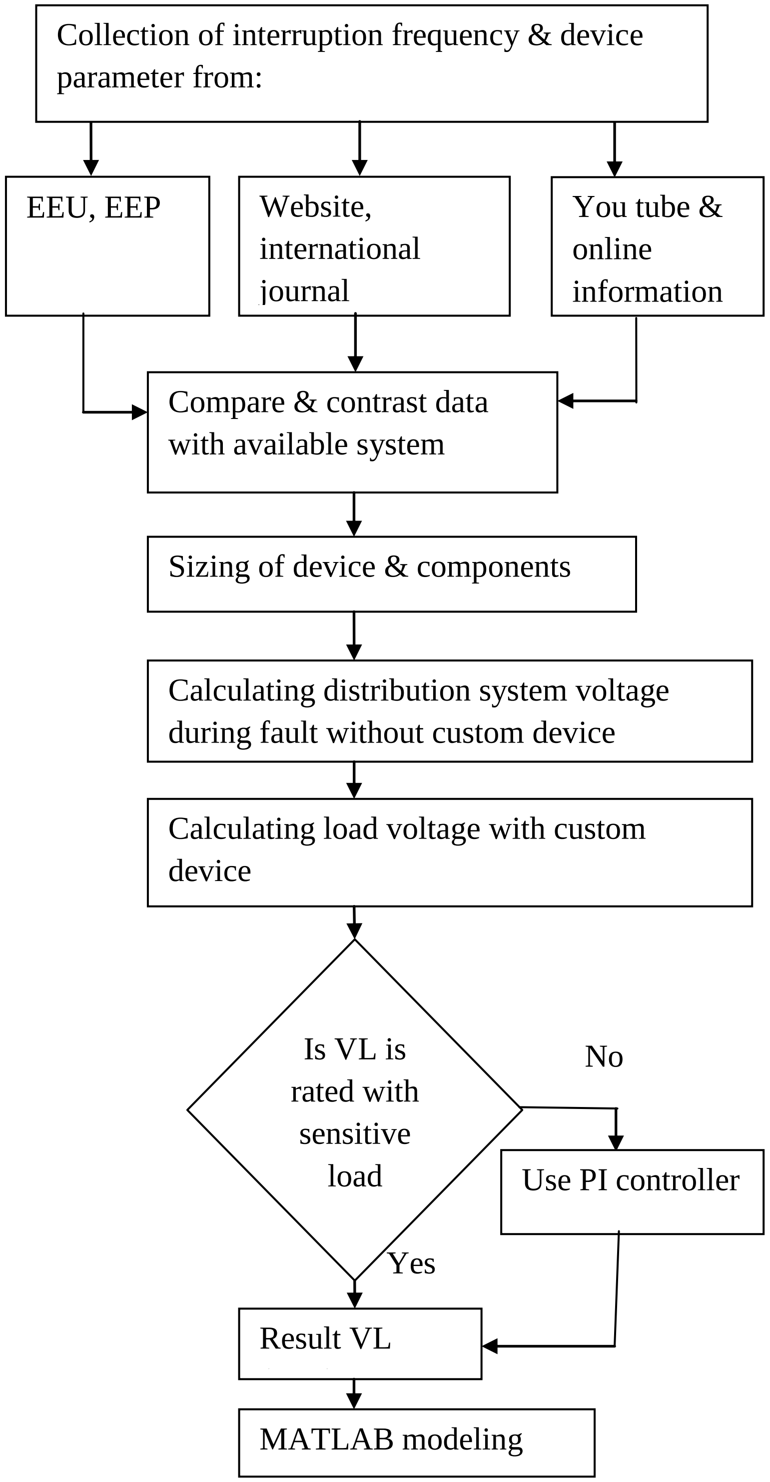

Figure 3.5: Conceptual framework of the study

3.2.2 Realization of Hawassa distribution system

The distribution system is the electrical system between the sub-station fed by the transmission system and the consumer meter. The general parts of the distribution system are, distributors and service mains.

I) **Feeders:** A feeder is a conductor which connects the sub-station (or localized generating station) to the area where power is to be distributed. Generally, no tapings are taken from the feeder so that current in it remains the same throughout. The main consideration in the design of a feeder is the current carrying capacity.

II) **Distributor:** A distributor is a conductor from which tapings are taken for supply to the consumers. The current through a distributor is not constant because tapings are taken at various places along its length. While designing a distributor, voltage drop along its length is the main consideration since the statutory limit of voltage variations is ± 6% of rated value at the consumers' terminals [16].

III) **Service mains.** A service main is generally a small cable which connects the distributor to the consumers' terminals.

As a general the sub-station of Hawassa city was done with the above concepts, it is illustrated in block diagram shown by ProfiCAD software in figure 3.6 below. The main equipments used in substation are:

I) **Bus bars -** When a number of lines operating at the same voltage have to be directly connected electrically, bus-bars are used as the common electrical component.

II) **Isolating switches.** In sub-stations, it is often desired to disconnect a part of the system for general maintenance and repairs.

III) **Power Transformers.** A power transformer is used in a sub-station to step-up or step-down the voltage.

IV) **Instrument transformers-** The lines in sub-stations operate at high voltages and carry current of thousands of amperes. The measuring instruments and protective devices are designed for low voltages and low currents. Therefore, they will not work satisfactorily if mounted directly on the power lines. This difficulty is overcome by installing instrument transformers on the power lines. There are two types of instrument transformers.

1. **Current transformer (C.T.) -** It is essentially a step-up transformer which steps down the current to a known ratio.
2. **Voltage transformer (V.T) -** It is essentially a step down transformer and steps down the voltage to a known ratio.

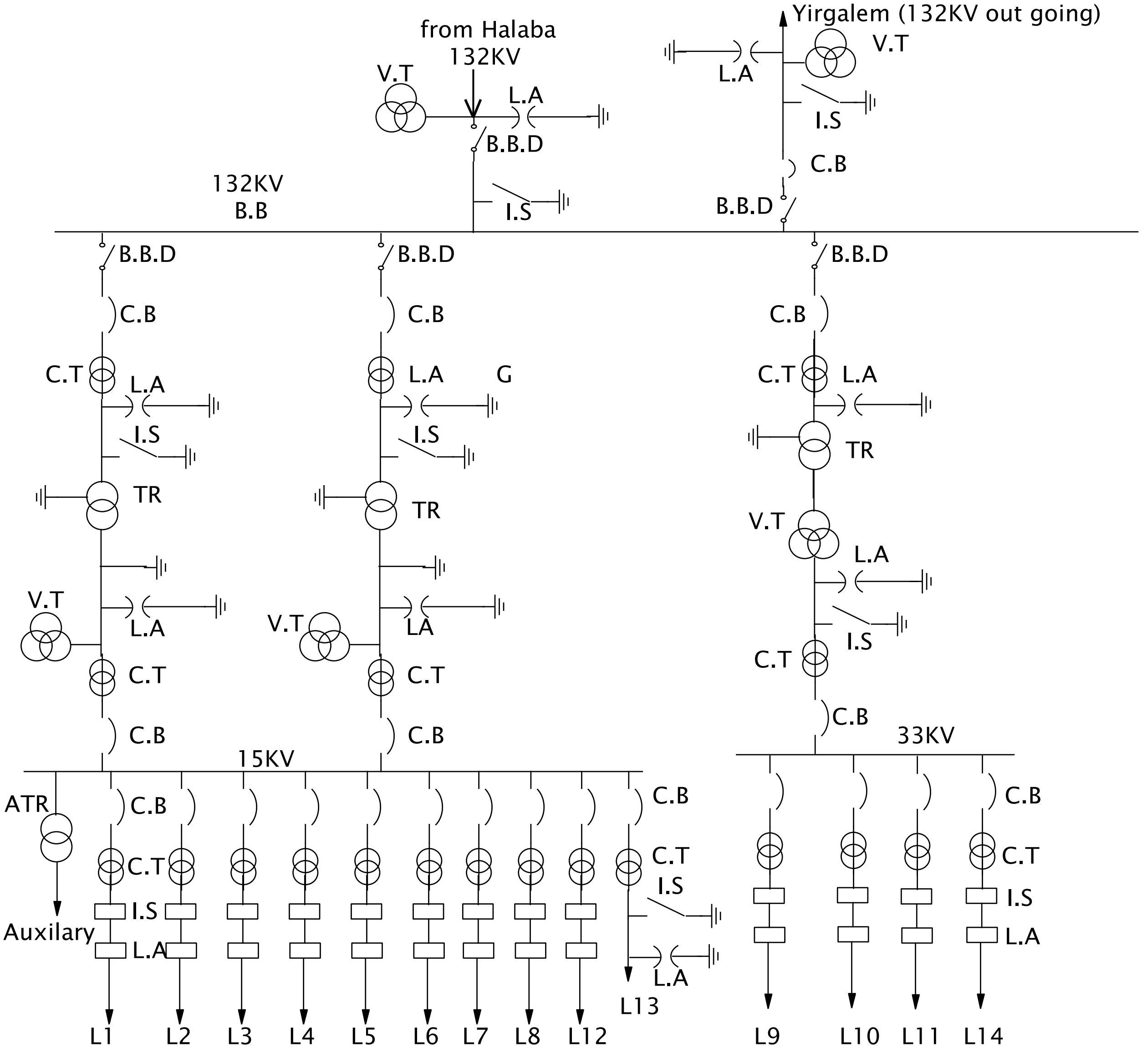

Figure 3.6 Hawassa city substation, feeder and distribution system block diagram

Legend:

I.S – Isolated switch
B.B.D- Bus bar disconnect
C.B- Circuit breaker
C.T- Current transformer
V.T- Voltage transformer
L.A- lightning arrester
ATR- Auxiliary transformer
TR- transformer
G-Ground

During load condition the maximum and minimum current of each of the feeder is described in table 3.1 below and from figure 3.6 feeder 2 is an idle.

Table 3.1: maximum and minimum current value of each feeder [24]

Line (L)	Maximum current (A)	Minimum current (A)	Voltage level(KV)
1	232	80	15KV
3	66	10	15KV
4	240	40	15KV
5	280	80	15KV
6	167	43	15KV
7	77	11	15KV
8	110	20	15KV
9	9	5	33KV
10	18	8	33KV
11	52	15	33KV
12	96	27	15KV
13	167	42	15KV
14	9	5	33KV

The mathematical expression to calculate the total load of each of the feeder is:

$$P = \sqrt{3}\ VI \cos\theta \tag{3.2}$$

The power quality is characterized in different categories depend on the duration of variation. From those according to IEEE 1159:1995 standard some of categories which related with this proposed are illustrated in table 3.2 below [7, 10]. And the permanent and temporary fault of frequency duration of Hawassa city distribution system was daily recorded at substation site as shown in table 3.3 (Appendix D1 and Appendix D2).

Table 3.2: power quality categories and its problem [7, 10]

Categories	Effect		Duration	Voltage magnitude(p.u)
Short duration variation	Instantaneous	Interruption	0.5-30 cycles	$<$ 0.1 pu
		Sag (dip)	0.5-30 cycles	0.1-0.9 pu
		Swell	0.5-30 cycles	1.1-1.8 pu
	Momentary	Interruption	30 cycles - 3 s	$<$ 0.1 pu
		Sag (dip)	30 cycles - 3 s	0.1-0.9 pu
		Swell	30 cycles - 3 s	1.1-1.2 pu
	Temporary	Interruption	3s - 1 min	$<$ 0.1 pu
		Sag (dip)	3s - 1 min	0.1-0.9 pu
		Swell	3s - 1 min	1.1-1.4 pu
Long duration variation	Under voltage		$>$ 1 min	0.8 - 0.9 pu
	Over voltage		$>$ 1 min	1.1 -1.2 pu

Table 3.3: Interruption data of Hawassa distribution in July, 2016 [24]

Line (L)	Pef /month	Psc/month	Tef/month	Tsc/month	Sol/month	Oper/month
1	1 - times	4 - times	2 - times	12 - times	No	9 - times
3	No	No	No	No	No	1 - times
4	4 - times	6 - times	2 - times	4 - times	No	12 - times
5	4 - times	4 - times	5 - times	12 - times	No	7 - times
6	6 - times	3 - times	6 - times	9 - times	No	10 - times
*7	No	3 - times	7 - times	14 - times	No	9 - times
8	No	2 - times	No	4 - times	No	1 - times
9	No	No	No	No	No	9 - times
10	13 - times	17 - times	4 - times	10 - times	No	11- times
11	No	2 - times	No	No	No	3 - times
12	6 - times	7 - times	7 - times	10 - times	No	13 - times
13	5 - times	4 - times	2 - times	11 - times	No	7 - times
14	1 - times	1 - times	No	No	No	3 - times

Where:

Pef- is permanent earth fault Tef- is temporary earth fault
Psc – is permanent short circuit Tsc- is temporary short circuit
Sol- is system over load Oper – is operational fault

The above table data is taken from Hawassa substation which is shown the monthly occurred system faults. Through in days or within a period of time there is fault occurring on each of the feeder. Even though as gathered the data some of the line are mostly occurring with the faults rather than others. This is due to the environmental problem, unbalanced load on a three phase system, equipments not suitable for local supply and switching of heavy load. So as shown in table 3.3 above line number seven “7” is familiar with this reason and it is selected as reference feeder in this paper to propose and to simulate by matlab/simulink software.

The source of power supply means 132KV is supplied from Halaba town which is connected at point of common coupling (PCC) to 33/15/15KV by Δ/Δ/Y.

But in this study it is proposed that at custom power source which is supplied from single 15/0.415KV connected by Δ/Y. The schematic diagram is drawn by ProfiCAD software in figure 3.7 below which shows the distribution system and the integration of UCAP-DVR connected in series to mitigate the power quality.

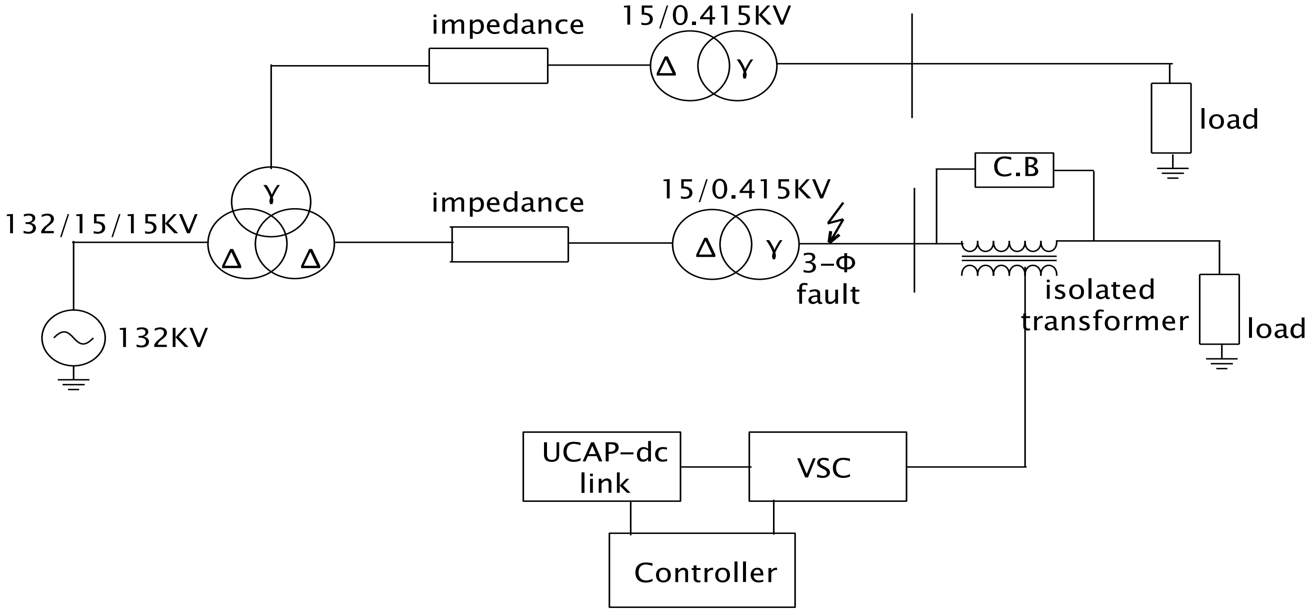

Figure 3.7: Schematic diagram of UCAP- DVR test system

The UCAP- DVR simulation with their controller is verified for voltage compensation of the fault occurring at the point of 3-ϕ fault sign shown at figure 3.7 with the specified fault resistance and time duration (i.e. explained in simulation result).

3.3 Method

3.3.1 Operating Principle of DVR

The basic function of the DVR is to inject a dynamically controlled voltage, V_{DVR} generated by a forced commutated converter in series to the bus voltage by means of a booster transformer. The momentary amplitudes of the three injected phase voltages are controlled such as to eliminate any detrimental effects of a bus fault to the load voltage (VL).

This means that any differential voltages caused by transient disturbances in the ac feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the booster transformer.

The DVR works independently of the type of fault or any event that happens in the system, provided that the whole system remains connected to the supply grid, i.e. the line breaker does not trip. For most practical cases, a more economical design can be achieved by only compensating the positive and negative sequence components of the voltage disturbance seen at the input of the DVR. This option is reasonable because for a typical distribution bus configuration, the zero sequence part of a disturbance will not pass through the step down transformer because of infinite impedance for this component. The DVR has three modes of operation which are: protection mode, standby mode, injection/boost mode.

I. Protection Mode

If the over current on the load side exceeds a permissible limit due to short circuit on the load or large inrush current, the DVR will be isolated from the systems by using the bypass switches (S2 and S3 will open) and supplying another path for current (S1 will be closed).see figure 3.8 below.

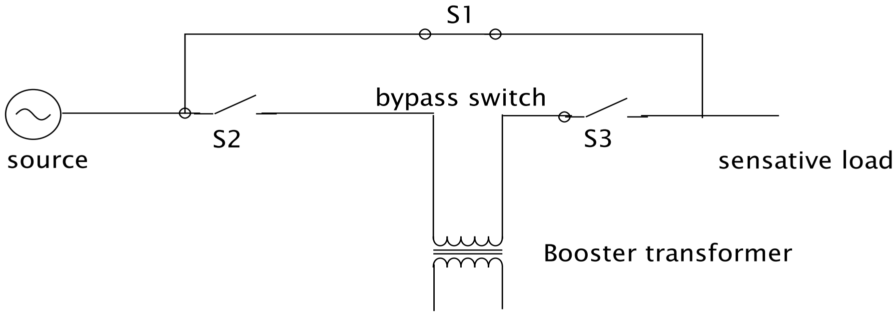

Figure 3.8: protection modes

II. Standby mode

In standby mode (VDVR=0), the booster transformer's low voltage winding is shorted through the converter. No switching of semiconductors occurs in this mode of operation, because the individual converter legs are triggered such as to establish a short-circuit path for the transformer connection. Therefore, only the comparatively low conduction losses of the semiconductors in this current loop contribute to the losses. The DVR will be most of the time in this mode, shown in figure 3.9 below.

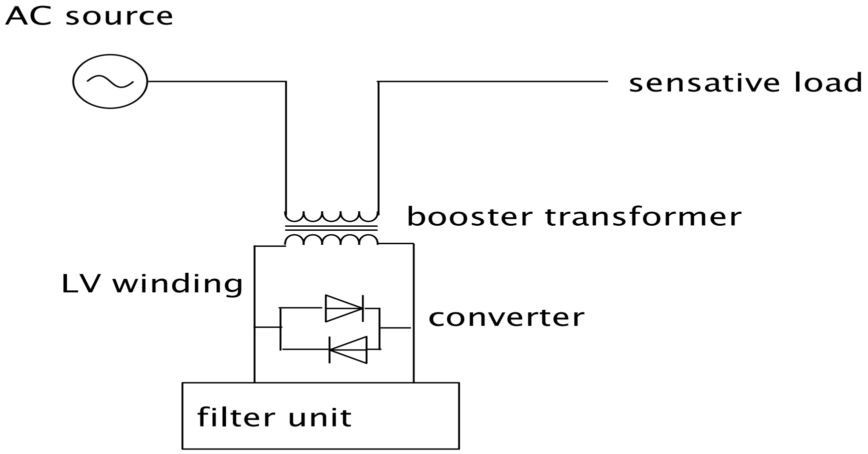

Figure 3.9: Standby modes

III. Injection/Boost Mode

In boost mode (VDVR>0), the Injection/Boost mode the DVR is injecting a compensating voltage through the booster transformer due to the detection of a disturbance in the supply voltage.

3.3.2 DVR Voltage Injection Methods

The possibility of compensating voltage sag can be limited by a number of factors including finite DVR power rating, different load conditions and different types of voltage sag. Some loads are very sensitive to phase angle jump and others are tolerant to it. Therefore, the control strategy depends on the type of load characteristics. There are three different methods for DVR voltage injection which are presented below.

I. Pre-Dip Compensation (PDC)

The PDC method tracks the supply voltage continuously and compensates load voltage during fault to pre-fault condition. In this method, the load voltage can be restored ideally, but the injected active power cannot be controlled and it is determined by external conditions such as the type of faults and load conditions. This method is achieved by using a fault detector to freeze the output from the Phase Locked Loop (PLL) circuit, when the fault occurs. Then, the frozen angle is used to restore the previous balanced load voltages by using the Park transform [21]. The lack of the negative sequence detection in this method leads to the phase-oscillation in the case of single-line faults. Figure 3.10 shows the single-phase vector diagram of this method.

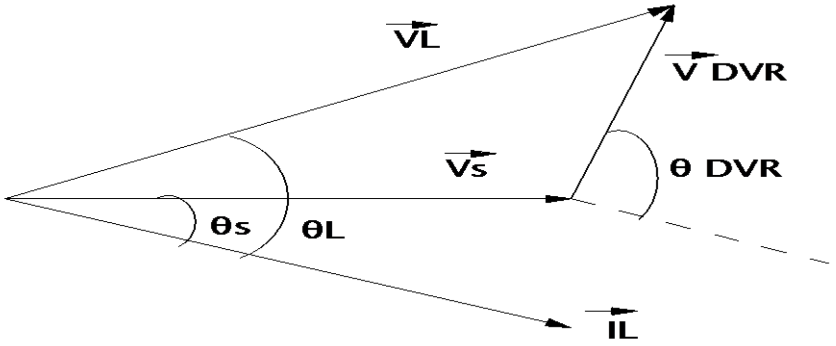

Figure 3.10: single-phase vector diagram of Pre-Dip Compensation method

According to Figure 3.10, the apparent power of DVR is:

SDVR = IL*VDVR (3.3)

$= I_L\sqrt{V_L^2 + V_S^2 - 2V_LV_SCOS(\theta L - \theta S)}$

And the active power of DVR is:

$P_{DVR}= I_L(V_L\cos\theta_l - V_s cos\theta_s)$

The magnitude and the angle of DVR voltage are:

$V_{DVR}=\sqrt{V_L^2 + V_S^2 - 2VLVScos(\theta_L - \theta_S)}$

$\theta_{DVR}=tan^{-1}(\frac{V_Lsin\theta_L - V_Ssin\theta_S}{V_L\cos\theta_l - V_scos\theta_s})$

II. In- Phase Compensation:

In this method, injection voltage is in phase with the source voltage [21]. When the source voltage is drop due to sag in the distribution network, then injection voltage produced by the Voltage Source Inverter (VSI) will inject the missing voltage according to voltage drop magnitude. The IPC method is suitable for minimum voltage or minimum energy operation strategies [18]. In other word, this approach requires large amounts of real power to mitigate the voltage sag, which means a large energy storage device.

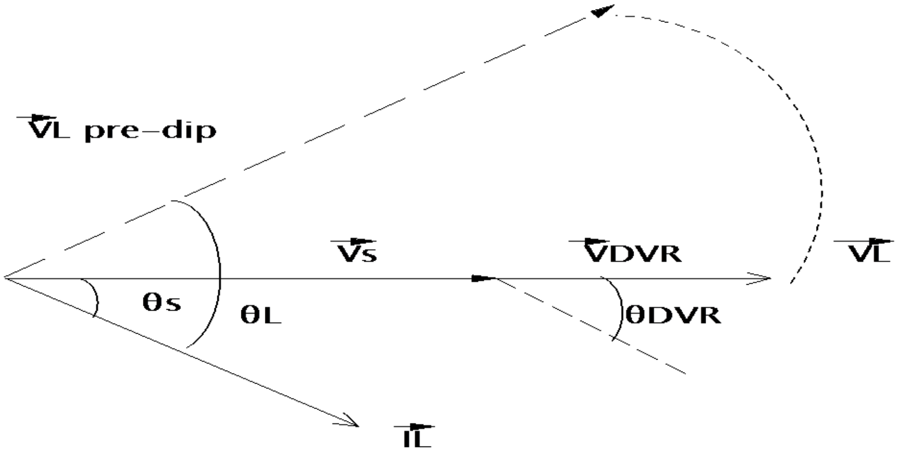

Figure 3.11: single-phase vector diagram of In- Phase Compensation

According to Figure 3.11, the apparent power of DVR is:

S_{DVR}=I_L *V_{DVR}= $I_L(V_L - V_S)$ (3.4)

And the active power of DVR is:

P_{DVR}=I_L*V_{DVR} cosθ_s = $I_L(V_L - V_S)$ cosθ_s

The magnitude and the angle of the DVR voltage are:

V_{DVR}=V_L - V_S , $\theta_{DVR} = \theta_S$

III. In Phase Advance Compensation (IPAC) or Minimum Energy Compensation

This method reduces the energy storage size. Reducing energy storage means that ride-through ability is increased when the energy storage capacity is fixed. Active power (P_{DVR}) depends on the angle α. The injection active power is made zero by means of having the injection voltage phasors perpendicular to the load current phasors. IPAC method should be adjusted to the load that is tolerant to phase angle jump, or transition period should be taken while phase angle is moved from pre-fault angle to advance angle.

In short, IPAC method uses only reactive power and unfortunately, not al1 the sags can be mitigated without real power, as a consequence, this method is only suitable for a limited range of sags. During the sag, phase of load voltage jump's a certain step that causes difficulties for load [18, and 21]. The magnitude of the restored load voltage that is maintained at pre-fault condition is shown in figure 3.12.

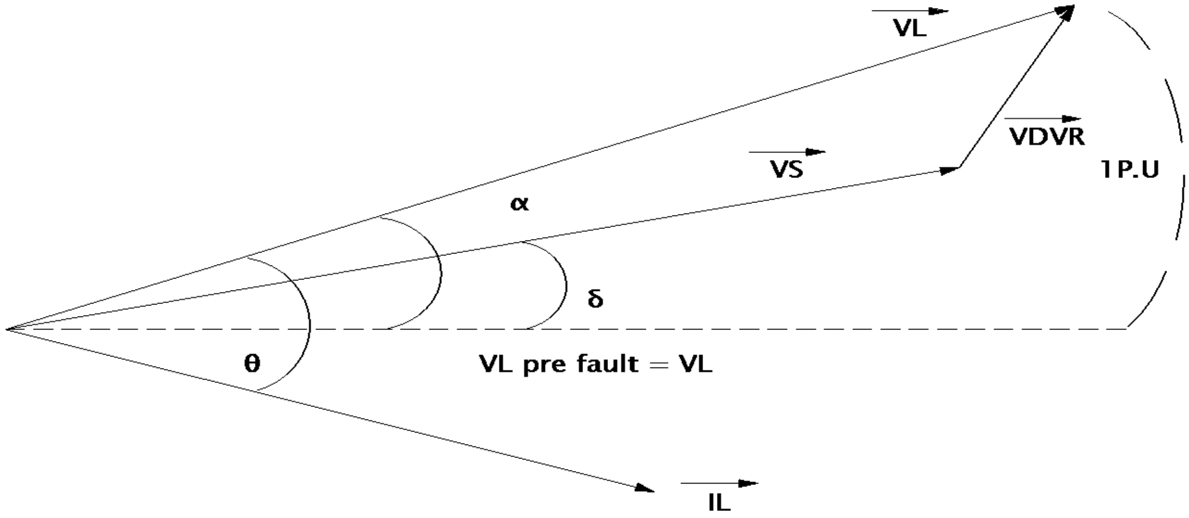

Figure 3.12: In Phase Advance Compensation diagram

3.3.3 Sizing of injection transformer

The appropriate KVA size of three phase Buck-boost transformer is determined by:

$$\text{Three- phase KVA} = \frac{\text{Load voltage x load current x}\sqrt{3}}{1000} \tag{3.5}$$

An electrical power and voltage are generally taken as base quantities in three phase system. Three phase power in MVA or KVA is taken as base power and line to line voltage in KV is taken as base voltage. The base impedance of the system can be calculated from these base power and base voltage as follows:

$$Zb = \frac{KV^2}{KVA} \text{ ohms} \tag{3.6}$$

From table 3.1 the maximum load current requirement for feeder number "7" is 77A and the actual load voltage is 415V. Therefore, the requirement apparent power of injection transformer is determined by using equation 3.5.

$$\text{Three- phase KVA} = \frac{\text{VL−L(V)x IL(A) x}\sqrt{3}}{1000}$$

Maximum ampere rating of the over current device = Full Load Input Amps X 125 percent.

But according to IEEE 141-1993 standard 75KVA 3-ɸ transformer has 2.42, 2.1 and 3.2 percent of resistance (%R), reactance (%X) and impedance (%Z) respectively. And From 15KV/0.415KV, 75KVA, 3-ɸ of feeder transformer we can calculate short circuit current (A), impedance transformer and voltage sag in per unit as follows:

Short circuit rms amperes at transformer terminals are calculated by per unit method (Appendix B).

$$\text{Ztrans} = \sqrt{(Xtrans)^2 + (Rtrans)^2} \tag{3.7}$$

$$\text{Isc} = \frac{KVA}{\sqrt{3}\, X\, VL{-}L\, X\, Ztrans} \tag{3.8}$$

From section 2.2.2 the most common type of fault is the single line to ground fault and the impedance fault is calculated from figure 2.2.

$V_A = I_A \times Z_{fault}$

$\text{Zfault} = \frac{VL(V)}{Isc(A)}$

$\text{Vsag} = \frac{\text{VL(V) X } Zfault}{Zfault + Ztrans}$

Vmissing = Vpresag – Vsag

We will assume that the pre-event voltage is exactly 1 p.u and consider a DVR compensated single phase system as shown in Figure 3.13. Let us assume that source voltage is 1.0 p.u and we want to regulate the load voltage to 1.0 p.u. Let us denote the phase angle between V_s and V_l as δ. Further we assume that during DVR operation, real power is not required except some losses in the inverter and the non ideal filter components. These losses for the time being are considered to be zero. This condition implies that the phase difference between V_{DVR} and I_s should be 90°. Let us first consider a general case to understand the concept. The DVR equivalent circuit with fundamental voltages and current is shown in Figure 3.13. Applying Kirchhoff's voltage law in the circuit,

$$V_s + V_{DVR} = I_s\,(\text{Rs} + \text{jXs}) + V_l = \text{Is Zs} + V_l \tag{3.9}$$

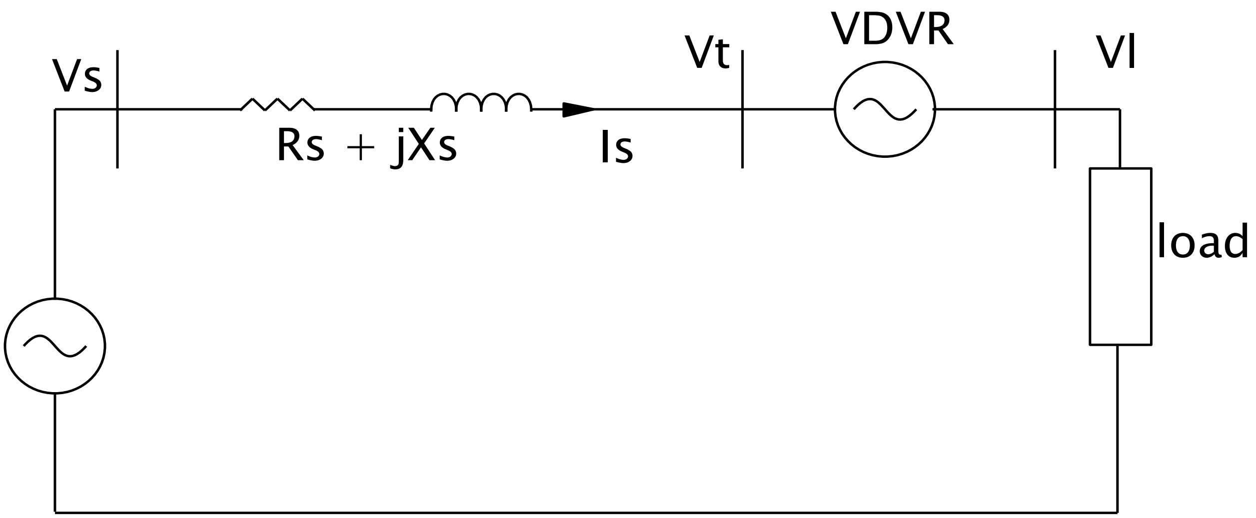

Figure 3.13: Schematic diagram of DVR based compensation in a distribution

Note that in above circuit I_s = I_l = I. The load voltage V_l can be written in terms of load current and load impedance as given below.

$$V_s + V_{DVR} = I\,(Zs + Z_l) \tag{3.10}$$

Using (3.9), the source voltage can be expressed as in the following.

$$V_s = V_l + I\,Rs - (V_{DVR} - jIXs)$$

With the help of above equation, the relationship between load voltages, the source voltages and DVR voltages can be expressed as follows.

$$V_l = \left(\frac{Vs + V_{DVR}}{Zs + Zl} \right) Z_l \tag{3.11}$$

From equation (3.11) Without DVR, the load terminal voltage V_l can be given as following.

$$I_l = \frac{Vs}{Zs + Zl}$$

$$V_l = I_l \; X \; Z_l$$

Now with DVR it is desired to maintain load voltage same as supply voltage in magnitude and phase angle. Thus, substituting $Vs = V_l$ in equation (3.9), we get,

$$Vs + V_{DVR} = I_s\,(\mathrm{Rs} + \mathrm{jXs}) + V_l$$

$$V_{DVR} = I_s\,(\mathrm{Rs} + \mathrm{jXs})$$

$$V_{DVR} = \frac{V_{l(\mathrm{Rs} + \mathrm{jXs})}}{Zl}$$

From figure (3.13) line current is computed as follows:

$$I_s = \frac{V_l}{Zl}$$

It is to be noted that, although Vs = V_l = $1\llcorner0^0$ p.u, it does not imply that no power flows from source to load. In fact the total effective source voltage is:

$V's = Vs + V_{DVR}$

By assuming during high load condition, which means during swell condition neglect line resistance and load resistance V_{DVR} become:

$$V_{DVR} = \frac{1\llcorner0^0(jXs)}{jXl}$$

$$V_l = (1\llcorner0^0 + V_{DVR}) \text{ p.u}$$

From section 3.3.2 the real power of DVR in phase compensation method is calculated as follows:

Since in phase compensation method $V_{DVR} = V_{sag}$

$P_{DVR} = V_{DVR}$ X $I_l \cos\theta_s$

$P_L = \cos\theta$ X KVA

$Q_L = \sin\theta$ X KVA

Since DVR can supply only limited amount of real power and is not able to compensate for higher values of PQ problems. This approach requires large amounts of real power to mitigate the voltage sag, which means a large energy storage device.

At 25MVA, 132KV/15KV, 3-ϕ of transformer we can calculate the reactance and resistance of transformer in per unit as follows:

According to IEEE 141-1993 standard 25MVA, 132KV/15KV, 3-ϕ transformer has X/R = 7 and %Z = 10.

$\tan\theta = \frac{X}{R} = 7, \ \theta = tan^{-1}(7)$

$\sin\theta = \frac{X}{Z}$

$\cos\theta = \frac{R}{Z}$

X = Z x $\sin\theta$

R = Z x $\cos\theta$

The back-boost transformer is characterized by decreasing and increasing voltage level which is rated according to “Dongan Company” [19] (appendix F).

3.3.4 IGBT sizing

At high power, inverters or converters typically use 'bridge' configurations to generate line-frequency AC or to provide bi-directional PWM drive to motors, transformers or other loads. Bridge circuits include IGBTs whose emitters are switching nodes at high voltage and high frequency so the gate drive PWM signal and associated drive power rails, which use the emitter as a reference, have to be 'floating' with respect to system ground, so called 'high side' drives.

Additional requirements are that the drive circuit should be immune to the high 'dV/dt' of the switch node and have a very low coupling capacitance.

The gate of an IGBT must be charged and discharged through Rg (internal and external gate resistance) in each switching cycle. If the IGBT data sheet provides a gate charge curve then the relationship is:

$$Pgd = Qg \times F \times Vs \qquad (3.12)$$

Where:

Pgd - is gate drive power

Qg - is data sheet charge for a chosen gate voltage swing,

Vs - is positive to negative voltage swing.

According to IEC 60747-9 data if we approximate the parameter from the IGBT data given below [20, 23]:

I_c = 200A, Vce = 150V, Vge = ±15 V, internal and external gate resistance is 2Ω respectively, Tc = 25^0c and Tj = 150 ^{0}c.

Where:

I_c - is collector current

Vce – is collector- emitter voltage

Vge – is gate emitter voltage

Tc – is case temperature

Tj – is junction temperature

If the data sheet does not provide a charge curve but just a Qg value at specific gate voltages, the value of Qg at other gate voltage swings can be approximated by multiplying by the ratio of the actual versus data sheet voltage swings [20]. Let see gate charge Qg value of 3.7 μC with ±15 V gate voltage swing (30 V total). For a swing of +15 to -9 V (24 V total) gate charge approximates to 3 μC.

In other case Pgd = E x Fsw

By substituting E = ½ x Qg x (Vgon - Vgoff)

Pgd = ½ x Qg x (Vgon - Vgoff) x Fsw

Therefore $\mathrm{Fsw} = \frac{2 \times \mathrm{Pgd}}{\mathrm{Qg} \times (\mathrm{Vgon} - \mathrm{Vgoff})}$ (3.13)

Where

Pgd – gate driver power

Qg – gate charge

Fsw – switching frequency

Tsw – switching period

The average charge and discharge current given by Pg/Vge is 30 mA.

The peak current Ipk, required to charge and discharge the gate is a function of Vge, gate resistance of the IGBT internal resistance Rg and external resistance Rg.

$\mathrm{Ipk} = \frac{\mathrm{V\,sw}}{\mathrm{Rgint} + \mathrm{Rgext}}$ (3.14)

Where

Ipk – peak current required to charge and discharge.

Vsw – gate voltage swing

Rgint – internal gate resistance

Rgext – external gate resistance

The total gate drive energy E per cycle is given by:

E = Qg x Vge

The bulk capacitors on the +15 and -9 V rails supply this energy in proportion to their voltages so the +15 V rail supplies 45 µJ. If we assume that the bulk capacitor on the +15 V rail should not drop more than say 0.5 V each cycle then we can calculate minimum capacitance "C" by equating the energy supplied with the difference between the capacitor energies at its start and finish voltages, that is;

$\mathrm{E} = \frac{1}{2}\mathrm{C}\ \left(V_{initial} - V_{final}\right)^{2}$ (3.15)

DC-DCs for high side IGBT drive the switched 'DC-link' voltage across their barrier. This voltage can be kilovolts with very fast switching edges from 10 kV/µs upwards. Latest gallium nitride (GaN) devices may switch at 100 kV/µs or more. This high 'dV/dt' causes displacement current through the capacitance of the DC-DC isolation barrier of value:

$I = C.\ dV/dt$ (3.16)

So for just 20 pF and 10 kV/µs, 200 mA is induced. This current finds an indeterminate return route through the controller circuitry back to the bridge causing voltage spikes across connection resistances and inductances. Potentially it disrupts operation of the controller and the DC-DC converter. Low coupling capacitance is therefore desirable, ideally less than 15 pF.

The maximum allowable power dissipation (Pdis) in the IGBT for a specific case temperature using the datasheet parameters is given by [21]:

$$\text{Pdis} = \frac{\Delta T}{Rth} = \frac{Tj - Tc}{Rth} \tag{3.17}$$

The size of the inverter should be required for this system is determined as follows:

$$\text{Size of inverter} = \frac{Total\ load + 20\% Al}{E\%} = \frac{Tl(1+20\%)}{E\%} \tag{3.18}$$

Where

Al – additional load 20% of total load

E% - efficiency of inverter (80%)

Total load – active power (actual load)

3.3.5 Select a tuned frequency and Capacitor bank sizing for filter

The filter is designed to be tuned to the 4.7th. This is a common choice of notch frequency since the resulting parallel resonant frequency will be located around the fourth harmonic, a harmonic frequency that is not produced by most nonlinear loads [13].

The filter size is based on the load reactive power requirement for power factor correction. The reactor size is selected to tune the capacitor to the desired frequency. However, depending on the tuned frequency, the voltage rating of the capacitor bank may have to be higher than the system voltage to allow for the voltage rise across the reactor.

The desired power factor for distribution system is 80 percent. Assumed that the net reactive power from the filter required to correct from 65 to 80 percent power factor can be computed as follows:

A shunt passive filter can be designed for this system and applied at a 415V source. The load power where the filter will be installed is approximately ($\sqrt{3}\ x\ Ix\ Vx\ p.f$) with a power factor of 0.8 lagging.

A) Reactive power demand for a 65 percent power factor would be

- PL x sin [COS^{-1} (0.65)] kvar

B) Reactive power demand for an 80 percent power factor would be

- PL x sin [COS^{-1} (0.8)] kvar

C) Required compensation from the filter:

- [PL x sin [COS^{-1} (0.65)] - PL x sin [COS^{-1} (0.8)]] kvar

D) For a nominal 415V system, the equivalent filter reactance X_{Filt} is determined by:

$$X_{Filt} = \frac{VL^2}{Q} \tag{3.19}$$

X_{Filt} - is the difference between the capacitive reactance and the inductive reactance at fundamental frequency:

$$X_{Filt} = X_{cap} - X_l \tag{3.20}$$

- For tuning at the 4.7th harmonic:

$$X_{cap} = h^2 X_l \tag{3.21}$$

Thus, the desired capacitive reactance can be determined by:

$$X_{cap} = \frac{X_{filt} h^2}{h^2 - 1} \tag{3.22}$$

- To achieve this reactance at a 415V rating, the capacitor would have to be rated.

$$Q_C = \frac{VL^2}{X_{cap}} \tag{3.23}$$

- Compute filter reactor size.

$$X_{Lfund} = \frac{X_{cap}}{h^2} \tag{3.24}$$

$$L = \frac{X_{L(fund)}}{2\pi \, x \, 50}$$

And harmonic frequency is given by:

$$F_h = \frac{1}{2\pi\sqrt{LC}} \text{ , where } F_h \text{ is 4.7 x 50Hz} \tag{3.25}$$

$$Ceq = \frac{1}{4\pi^2 (Fh)^2 L}$$

- The apparent reactance of the combined capacitor and reactor at the fundamental frequency is:

$$X_{fund} = |X_{Lfund} - X_{cap}|$$

- The fundamental frequency filter current is:

$$I_{fund} = \frac{V_{actual}}{\sqrt{3} \, x \, X_{fund}} \tag{3.26}$$

- The fundamental frequency operating voltage across the capacitor bank is:

$$V_{L-Lcap} = \sqrt{3} \text{ x } I_{fund}\ x\ X_{cap} \quad (3.27)$$

This is the nominal fundamental voltage across the capacitor. It should be adjusted for any contingency conditions (maximum system voltage), and it should be less than 110 percent of the capacitor rated voltage. Because of the fact that the filter draws more fundamental current than the capacitor alone, the actual reactive power produced is larger than the capacitor rating:

$$Q_{Var(fund)} = \sqrt{3} \text{ x } I_{fund}\ x\ V_{actual} \quad (3.28)$$

3.3.6 Sizing of bidirectional DC-DC converter mode with ultra capacitor

From IGBT designing parameter data 'Vce' of IGBT switch device is 150V [23], which is become 300V for two IGBT switches taken as initial dc-link voltage and the inverter output voltage requirement is 415V. The duty cycle of bidirectional DC-DC converter is determined from equation (3.1) as follows.

$$\mathrm{D} = \frac{\mathrm{Vout-Vin}}{\mathrm{Vout}}$$

Also if we adjust our duty cycle at 'D' for bidirectional DC-DC converter switch, the voltage at DC-storage device can be calculated as follows:

$$\mathrm{Vdc} = \frac{1}{1-\mathrm{D}} V_c \quad (3.29)$$

Where Vdc – dc-link voltage

V_c - Voltage at ultra capacitor/storage device

- **Equivalent Capacitance of Ultra Capacitor bank**

To interface the higher voltage and proper energy storage capacity the ultra capacitor should be connected in series and parallel combination.

Generally the number of the series connected cells (N_s) in one branch are imposed by the rating of ultra capacitor cell at maximum voltage available in the market [22]. So it expressed as follows.

$$N_s = \frac{V_{max}}{V_{cell}} \quad (3.30)$$

Where:

N_s- are number of cell connected in series.

V_{cell}- is rating of ultra capacitor cell

The number of parallel branch (N_p) in the ultra capacitor bank can be given as:

$$N_p = \frac{N_S \text{ x } C_{eq}}{C_{cell}} \quad (3.31)$$

Where:

C_{eq} - is equivalent capacitance of ultra capacitor in farad

C_{cell} - is capacitance of each cell in farad

From number of series and parallel cell combination the total number of cell (N_T) required in ultra capacitor is given as follows:

$$N_T = N_p \ x \ N_S$$

- **Equivalent Series Resistance (ESR) of Ultra Capacitor bank**

When designing the ultra capacitor energy storage bank numbers of ultra capacitor cell are connected in series and parallel there by total series resistance of bank increase is called equivalent series resistance of the bank. It is expressed by the following formula.

$$R_{eq} = \frac{R_S \ x \ N_S}{N_p}$$

Where:

R_{eq}-is equivalent series resistance of ultra capacitor bank in ohm

R_s - is series resistance of each cell in ohm

The maximum energy stored in ultra capacitor is depends on its equivalent capacitance.

$$E_{max} = \text{P x t} = \frac{1}{2}(C_{eq} \text{ x } V_{max}^2) \quad (3.32)$$

From the above equation we can conclude that if the discharge time is increase the total capacitance requirement is increase. According to IEEE 1159-1195 and IEEE 519-1992 standards a typical duration of voltage sag and swell is 10 ms to 1 minute. So for the temporary fault of the system let say for the duration of 10msec, 1sec, 5sec and 1min the equivalent capacitance needed to mitigate the missing voltage is determined as follows:

From equation (3.32) the total load requirement is P (kW) which used as a reference to decide the total capacitance.

For a period of 10msec:

$$\text{Ceq} = \frac{2 \ x \ P \ x \ T_{10ms}}{Vmax^2}$$

To determine the total number of capacitor it's connected in series to increase the voltage value.

Total number of Ultra Capacitor connected in series (Cs) = $\frac{\text{Vmax}}{\text{Vcell}}$

The rated capacitor (C) value = Ceq (F) X Cs

For a period of 1sec:

Ceq = $\frac{2 \text{ x P x } T_{1s}}{\text{Vmax}^2}$

For a period of 5sec:

Ceq = $\frac{2 \text{ x P x } T_{5s}}{\text{Vmax}^2}$

For a period of 1min:

Ceq = $\frac{2 \text{ x P x } T_{60s}}{\text{Vmax}^2}$

Therefore in this study to rate useful energy (E), percentage of discharge (%d) and power (P), the duration of discharge is proposed within 5 second.

$$\%d_{min} = \frac{\sqrt{R_{eq}\ x\ P_d}}{V_{max}} \text{ x } 100$$

$$V_{min} = R_{eq} \text{ x } I_d = \sqrt{R_{eq}\ x\ P_d}$$

$$I_d = \sqrt{\frac{P_d}{R_{eq}}}$$

$$V_{min} = R_{eq} \text{ x } I_d$$

$$\%d_{max} = \frac{\sqrt{R_{eq}\ x\ P_d}}{V_{min}} \text{ x } 100 \approx 100$$

Useful energy and maximum energy are determined depend on the proposed duration of discharge.

$$E_{usefull} = \frac{1}{2}\ x\ C_{eq}(V_{max} - V_{min})^{\ 2}$$

$$E_{max} = \frac{1}{2}\ x\ C_{eq}(V_{max})^{\ 2}$$

The maximum power withdrawn from the ultra capacitor bank for duration of 5 second is:

$$E_{max} = P_{max} \text{ X } T_{5s}\ , P_{max} = \frac{E_{max}}{T_{5s}}$$

The maximum rated capacity (Ah) for a period of 5sec = $\frac{E_{max}(\text{KWS})}{Vc(V)}$

The rated capacity (Ah) during discharge for a period of 5sec = $\frac{E_{usefull}\ (\text{KWS})}{Vc(V)}$

3.3.7 Analysis of Proportional and Integral Controller

The Proportional-Integral (PI) controller mode is obtained from the combination of the proportional and the integral mode. In a parallel PI controller, the proportional and integral actions occur independently of each other, so the controller's variable (CV) output is equal to the proportional action plus the integral action. Equations for the proportional mode and integral mode are combined, to have an analytic expression for this mode, which is given below:

$CV_{new} = K_p e_p + K_i \int e_p d_t + CV_{t(0)}$ ………. (3.33)

$CV_{new} = K_p e_p + \frac{1}{ti} \int e_p d_t + CV_{t(0)}$

Where

$CV_{t(0)}$ Is Integral term value at t = 0 (initial value)

e_p Is the error

K_p Is proportional gain

K_i Is integral gain factor

ti Is integral time

The proportional gain, by design, also changes the net integration mode gain, but the integration gain, can be independently adjusted.

It is understood that the proportional offset occurred, when a load change required a new nominal controller output, and this could not be provided except by a fixed error from the set point. In the present mode, the integral function provides the required new controller output, thereby allowing the error to be zero after a load change. The integral feature effectively provides a 'reset' of the zero error output, after the load change occurs. At time t_1 a load change occurs, that produces the error. The accommodation of the new load condition requires a new controller output. The controller output is provided through a sum of proportional plus integral action that finally leaves the error at zero. The proportional part is obviously just an image of the error.

When the error is zero, the controller output is fixed at the value that the integral term had. This output is given by $CV_{t(0)}$ simply because we choose to define the time at which observation starts, as t = 0.

If the error is not zero, the proportional term contributes a correction and the integral term begins to increase or decrease the accumulated value [initial $CV_{t(0)}$], depending on the sign of the error and its direct or reverse direction. The integral term cannot become negative; thus it will saturate at zero, if the error and the action try to drive the area to a net negative value. The transfer function is given by K_p + (KI/s).

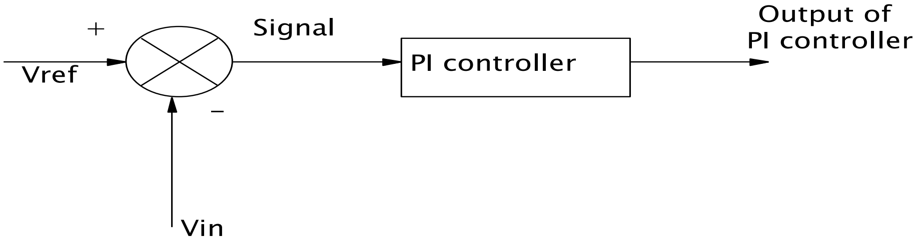

Figure 3.14: PI controller block diagram

In Proportional plus Integral Control action the actuating signal consists of proportional error signal with integral of the error signal. The block diagram is shown below figure 3.15

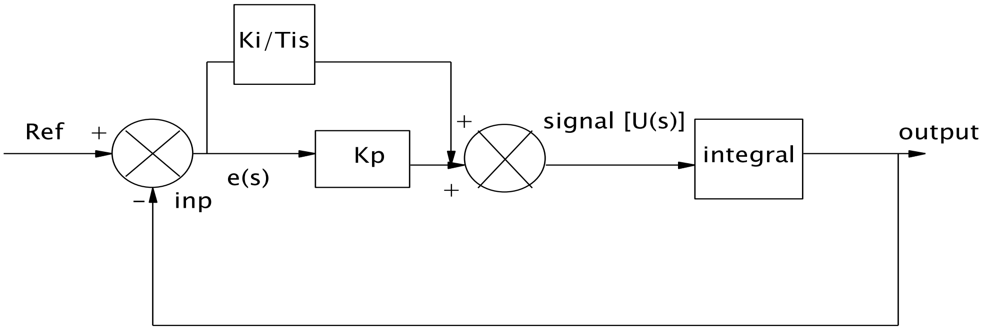

Figure 3.15: proportional plus integral block diagram

K_p and ti are constant and can be adjusted to any required values. Any change in K_p will affect both the actions i.e. propositional and integral control of the controller while change in ti would affect only the integral control action.

Sag occurs when there is increase in load or during the occurrence of fault and swell occurs when there is a sudden removal of load or due to addition of capacitor banks. This sag or swell in load voltage is sensed and its magnitude is compared with a reference voltage and the error. Signal is given to the PI controller as shown in Figure 3.15. The output of error detector is given by V_{Ref} - V_{in} shown above in figure 3.14.

Where:

V_{Ref} Is the reference voltage and V_{in} is the load voltage.

The PI controller processes the error signal and generates the required angle δ to drive the error to zero, for example; the load rms voltage is brought back to the reference voltage. The modulating angle δ or delta is applied to the PWM generators in phase A, whereas the angles for phase B and C are shifted by 240° or -120° and 120° respectively is explained in matlab software. .

$V_A = \sin(\omega t + \delta)$

$V_B = \sin(\omega t + \delta - 2\pi/3)$

$V_C = \sin(\omega t + \delta + 2\pi/3)$

The reason for PI controller selection is due to the fast response of changes to error variation. Integral action is slower than the proportional response but used to remove the offsets between the input and the reference at steady state. Before the DVR starts injecting voltage to the system, a considerable time period was allowed for the synchronization. The synchronization process was made according to the possible system frequency deviation. As the system frequency is not much deviate from 50 Hz the fast synchronization is not a necessity. Hence it helps the load voltage without phase jump.

The difference between load voltage (Vin) and reference voltage (Vref) is supplied to the PI controller. From the controller, the voltage magnitude is taken as feedback. The IGBT inverter is triggered from the pulse generated by the PWM generator. The IGBTs are triggered depending on the firing angle, δ, which introduces additional lag or lead in the voltage.

4 .RESULTS AND DISCUSSION

As discussed in section 3.3.3 the rate of injection transformer and distribution transformer are determined separately. In this study injection transformer is used as custom power device and the nominal voltage is dip with 168.2V or reduced by 70.08% of actual load voltage during fault condition. This result may be changed if the fault location is changed. Depend on the available load the apparent power of injection transformer was rated at 75KVA, which is equal with available distribution transformer.

During single phase to ground fault at available distribution transformer the missed voltage and voltage sag was calculated. So in order to inject the missed voltage injection transformer is supplied from the storage device via inverter with 415V AC. That means UCAP is deliver 216.8V of DC-voltage, which is used as an input for DC-DC converter. Then at DC- link the output of DC-DC converter was rated at 300V of DC- voltage. This fixed DC- link voltage is inverted to injection transformer to mitigate the missed load voltage from distribution line.

As a general the size of transformer and their parameter are specifically described in table 4.1 below:

Table 4.1: Size of Transformers and their parameter

Parameter	Injection transformer	Distribution transformer	Substation transformer
Rated voltage (V)	415	15,000/415	132,000/15,000
Power (KVA)	75	75	25,000
X (p.u)	0.021	0.024	0.0989
R (p.u)	0.0242	0.0242	0.01417
Z (p.u)	0.032	0.034	0.1
Zf (p.u)	0.073	0.078	_
Missing voltage (V)	168.2	167.14	_
Vsag (V)	71.8	72.86	_
Short circuit current(A)	3260.6	3061.37	_
phase	3-ϕ	3-ϕ	3-ϕ

According to IEC 60747.9 IGBT parameter standards data the switching frequency (Fsw) and switching period (Tsw) of the IGBT switching device was calculated. And also depend on the case temperature and junction temperature the maximum allowable power of IGBT was calculated, which is shown in table 4.2 below.

The filter system is designed by connecting capacitance and inductance in parallel to convert the inverted PWM wave form into sinusoidal wave form. Their rated value is shown in table 4.2 below.

The capacitance of Ultra capacitor which used as energy storage was designed for discharge duration of 5 seconds rated at 761F of capacitance and the equivalent capacitance is become 9.4F. But according to Maxwell technology the related UCAP available on the market is 800F, 2.7V per cell, equivalent series resistance of less than 1mΩ, leakage current of 1.5mA and current rate of 70A.

The input DC voltage required for this study is designed to 216.8V and 81 UCAP cell is connected in series to supply such amount of DC voltage. Depend on the equivalent series resistance, current rate of UCAP and time duration of discharge the required maximum energy and maximum power for this proposed was calculated and shown in table 4.2 below.

The missed voltage and voltage sag during single phase to ground fault without using custom power device is 0.696p.u and 0.304p.u respectively. The DVR voltage was designed at 0.705p.u to mitigate the missed voltage and also shown in terms of percentage and voltage measurements in table 4.2 below.

Table 4.2: Size of components and their parameter

<table>
<tr><td rowspan="2">Switching Device (IGBT)</td><td colspan="2">Fsw</td><td colspan="2">Tsw</td><td>I c</td><td>VCE</td><td>Vge</td><td colspan="2">Qg</td><td>Pdis</td></tr>
<tr><td colspan="2">16 KHz</td><td colspan="2">62.5µs</td><td>200A</td><td>150V</td><td>±15 V</td><td colspan="2">3 µC</td><td>1.5KW</td></tr>
<tr><td rowspan="2">Filter</td><td colspan="2">X_{cap}</td><td colspan="2">Q_C</td><td>L</td><td>Ceq</td><td>F_h</td><td colspan="2">V_{L-Lcap}</td><td>I_{fund}</td></tr>
<tr><td colspan="2">25.5Ω</td><td colspan="2">6.75$Kvar$</td><td>3.67mH</td><td>125µF</td><td>235Hz</td><td colspan="2">432.8V</td><td>9.8A</td></tr>
<tr><td rowspan="2">UCAP</td><td>Ceq</td><td colspan="2">Rated capacitor</td><td>UCAP voltage /cell</td><td>Duration of time</td><td>Req</td><td>%d_{min}</td><td>% d_{max}</td><td>E_{max}</td><td>P_{max}</td></tr>
<tr><td>18.8F</td><td colspan="2">761F</td><td>2.7V</td><td>5sec</td><td>40.5mΩ</td><td>19.5</td><td>≈ 100</td><td>441.8 KWs</td><td>88.36 KW</td></tr>
<tr><td rowspan="2">Vmissed with Out DVR</td><td colspan="2">(V)</td><td colspan="2">p.u</td><td colspan="6">Percentage</td></tr>
<tr><td colspan="2">167.14</td><td colspan="2">0.696</td><td colspan="6">69.6%</td></tr>
<tr><td>Vsag with Out DVR</td><td colspan="2">72.86</td><td colspan="2">0.304</td><td colspan="6">30.4%</td></tr>
<tr><td rowspan="2">Vswell</td><td colspan="2">(V)</td><td colspan="2">p.u</td><td colspan="6">Percentage</td></tr>
<tr><td colspan="2">270</td><td colspan="2">1.125</td><td colspan="6">112.5%</td></tr>
<tr><td rowspan="2">V_{DVR}</td><td colspan="2">(V)</td><td colspan="2">p.u</td><td colspan="6">Percentage</td></tr>
<tr><td colspan="2">169.2</td><td colspan="2">0.705</td><td colspan="6">70.5</td></tr>
<tr><td rowspan="2">DC-DC convertor</td><td colspan="2">duty cycle (D)</td><td colspan="2">Input DC-source</td><td colspan="6">dc-link voltage</td></tr>
<tr><td colspan="2">0.277</td><td colspan="2">216.8V</td><td colspan="6">300V</td></tr>
<tr><td rowspan="2">Inverter</td><td colspan="2">Vdc input (V)</td><td colspan="2">Vac output (V)</td><td colspan="6">Size of inverter (KW)</td></tr>
<tr><td colspan="2">300</td><td colspan="2">415</td><td colspan="6">66.5</td></tr>
<tr><td rowspan="2">PI controller</td><td colspan="4">Proportional gain (Kp)</td><td colspan="2">Integral gain (Ki)</td><td colspan="4">Integral time(Ti)</td></tr>
<tr><td colspan="4">1.2269</td><td colspan="2">1.76/msec</td><td colspan="4">0.00056 sec</td></tr>
</table>

The above all parameter are included in the matlab/simulink block diagram of UCAP-DVR integration in figure 4.1.

To overcome the power quality by using integration of UCAP-DVR it's simple to operate, the excellent solution for temporary fault and it's environmentally friendly. Since to implement the integration of UCAP-DVR for each of the feeder initially it may be high cost. Although now days in our country at most power distribution system there is no availability of custom device for protection of sensitive device and controller to mitigate the missing voltage during short period of fault occurring.

So even if it's may be initially high cost but if we consider the effect of system disturbance or power quality problem it become the better solution. In addition to improving the power quality problem there is also the advantageous of monthly profit for EEP. let consider the feed in tariff of the feeder " 7" without any fault in one month and with the temporary fault in one month. According to table 3.4 data the temporary earth fault and temporary short circuit fault in one month are 21 times. So if the fault is occurring for a period of 5 second and due to this fault if operational fault is taking average of 5hr in one month the feed in tariff is calculated as follows (Appendix D1 and D2). The agreement tariff rate of EEU for commercial at 15KV is 0.4088birr/kwh.

- Without system fault: by assuming if the system is operated for 24hr/ month.

Feed in tariff = P_L X 24hr/day X 30day/month X 0.4086birr/kwh

= 60kw X 24hr/day X 30day/month X 0.4086birr/kwh = 17,651.52birr/month

- With system fault:

The temporary fault in one month of feeder "7" is 21 times. If we consider for a period of 5 second, 5sec X 21 is become 105sec.

The total period of fault per month is therefore 105sec/3600sec/hr + 5hr/ month (operational fault) = 5.03hr /month.

24hr/day X 30day/month = 720hr/ month.

So the reduced system operated per one month is:

= (720 - 5.03) hr / month = 714.97hr/ month.

Feed in tariff = 60kw X 714.97hr/ month X 0.4086birr/kwh = 17528.3birr/month.

The reduced birr per a month = 17,651.52birr/month - 17528.3birr/month= 123.22birr/month.

The annual profit = 123.22birr/month X 12 month/year = 1478.64 birr/year.

4.1 Simulation result

The matlab/simulink block diagram of integrated UCAP-DVR is shown in figure 4.1; the simulation was done without UCAP-DVR connection and with UCAP-DVR connection to three phase distribution line.

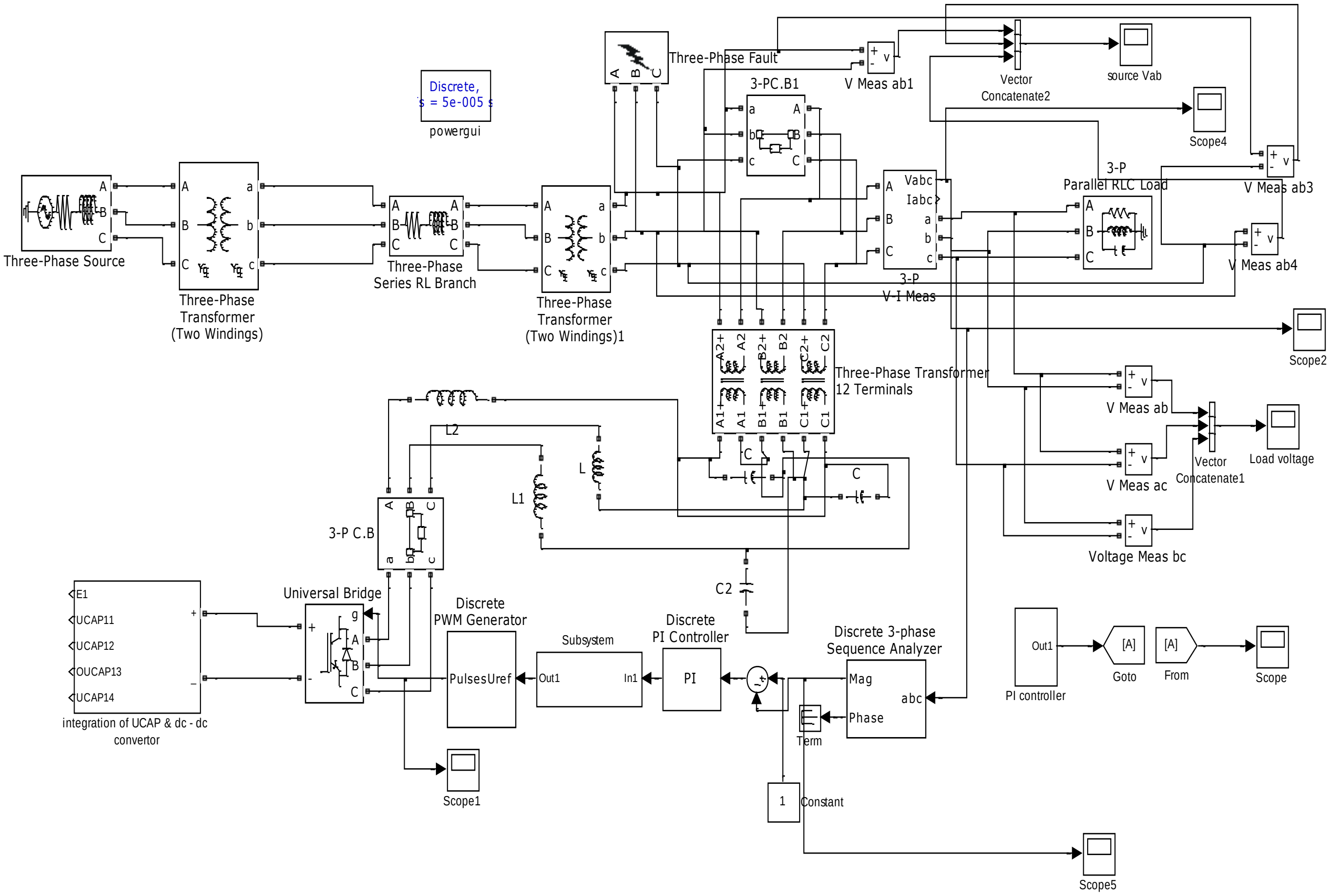

Figure 4.1: Matlab/simulink block diagram of integrated UCAP - DVR with distribution system

In figure 4.1 above the main three phase source is transmitted from Halaba substation at 132KV phase to phase voltage and at frequency of 50Hz. 132KV is reduced to 15KV via three phase transformer which is available at Hawassa substation. Then for the user 15KV is converted to low voltage at 415V by distributor transformer. In figure 4.1 above the fault sign block is connected to three phase line at low voltage side with fault resistance of 0.073 Ω. The UCAP-DVR integration is connected in series between sensitive load and distribution transformer to mitigate the missed voltage during fault occurring. The block “integration of UCAP and DC-DC converter” shown in figure 4.1 has the model of UCAP with bidirectional DC-DC converter circuit.

The firing angle pulse generated by PWM generator simulation was done. This is shown in Figure 4.2.

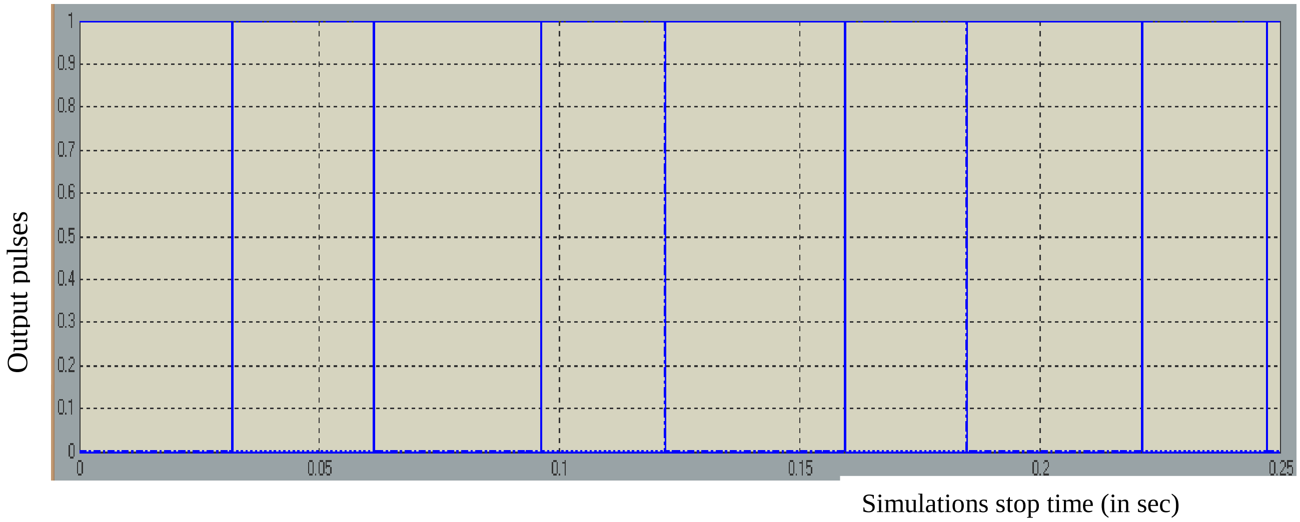

Figure 4.2: The firing angle pulse generated by PWM generator signal

In this proposed the obtained simulation results are included to illustrate and understand the performance of integration of UCAP-DVR under single-phase and three-phase voltage sags conditions. The simulation studies have been carried out using MATLAB / Simulink software as shown in figure 4.1. The configuration of the studied test system is as shown in Figure 3.7. The test system is comprised of a three-phase voltage source of 15 /0.415 kV at 50 Hz which feed a sensitive load. The inverters have been controlled using pulse width modulation generator with a fall time (Tf) $1e^{-6}$ seconds (s) and tail time (Tt) $2e^{-6}$ in seconds (s). The load considered in this study is with phase to phase nominal voltage of 415V, nominal frequency (FN) of 50Hz and reactive power of 45kVar.

Figure 4.3 below presents the results of simulation when a phase to ground resistive fault occurs, with a fault resistance equal to 0.073 Ω. The fault is produced at the low-voltage (LV) side of the distribution transformer. It starts at 0.0667s and lasts at 0.15s. Observe that the UCAP-DVR quickly injects the necessary voltage components to maintain the load voltage. The load voltage during fault with UCAP-DVR, without integration of UCAP-DVR and the injected voltage is shown figure 4.3, 4.4 and 4.5 respectively. In figure 4.3 below the load voltage sin wave is simulated with a three phase fault of starting from 0.0667s to 0.15s and the phase to ground voltage is sag/dip up to 30.4 % (0.304p.u) of its nominal value.

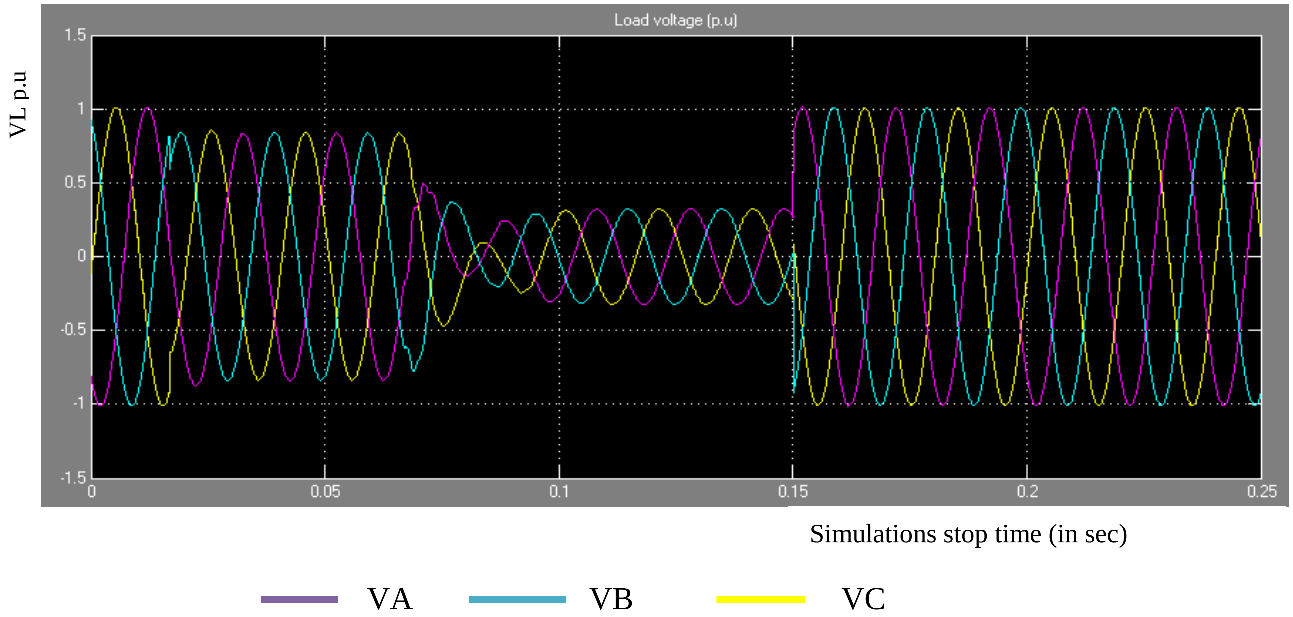

Figure 4.3: Simulation waveforms for voltages sag

During system fault without using any custom device to improve the power quality the output load voltage of the proposed distribution system is reduced by 0.696p.u or at 69.6% of the nominal voltage. The simulation result of output load voltage during fault without integration of UCAP-DVR is shown in figure 4.4 below.

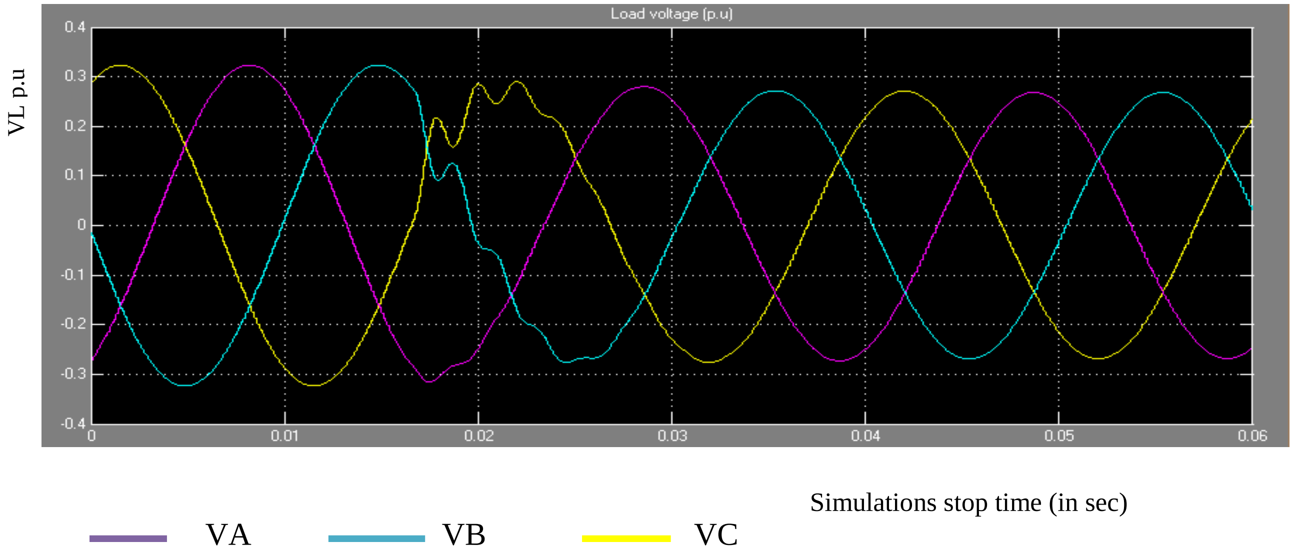

Figure 4.4: Load voltages during sag, without UCAP-DVR

Without released energy from storage device the injection transformer inject the voltage of [VinjA, VinjB and VinjC] for the voltage sag up to 1p.u for a period of 0.0667s to 0.15s is shown in Figure 4.5 below.

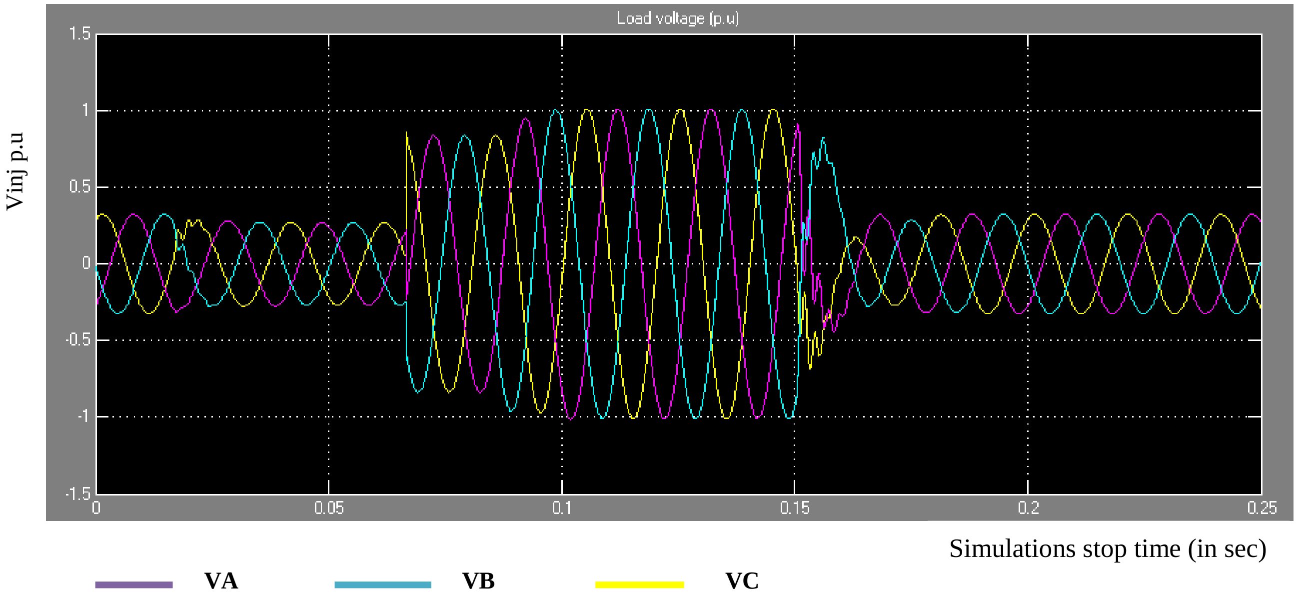

Figure 4.5: Injected voltages [VinjA, VinjB and VinjC] during voltage sag.

During system fault the voltage source is supplied from UCAP energy storage device to compensate output load voltage at 1p.u. By integrating UCAP with DVR device the compensated output load voltage simulation result is shown in figure 4.6 below.

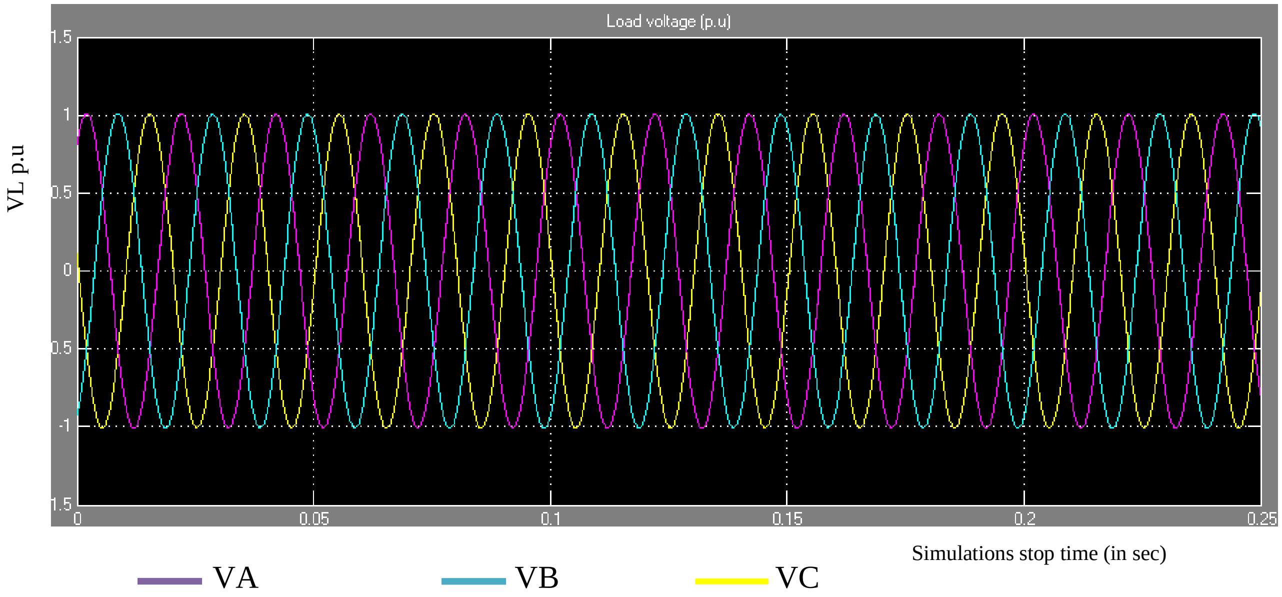

Figure 4.6: Compensated of load voltages, with UCAP-DVR

From Matlab/Simulink block diagram figure 4.1 above the sensitive load device is made up of a resistance connected in parallel with an inductance and capacitance. To verify the simulation result, by neglecting line resistance and load resistance from these sensitive load device the load voltage is increased from 1p.u to 1.125p.u for duration between 0.0667s to 0.15s. So it represents the voltage swell is increased to 112.5% of the nominal voltage. The simulation result of the voltage swell is shown in figure 4.7 below.

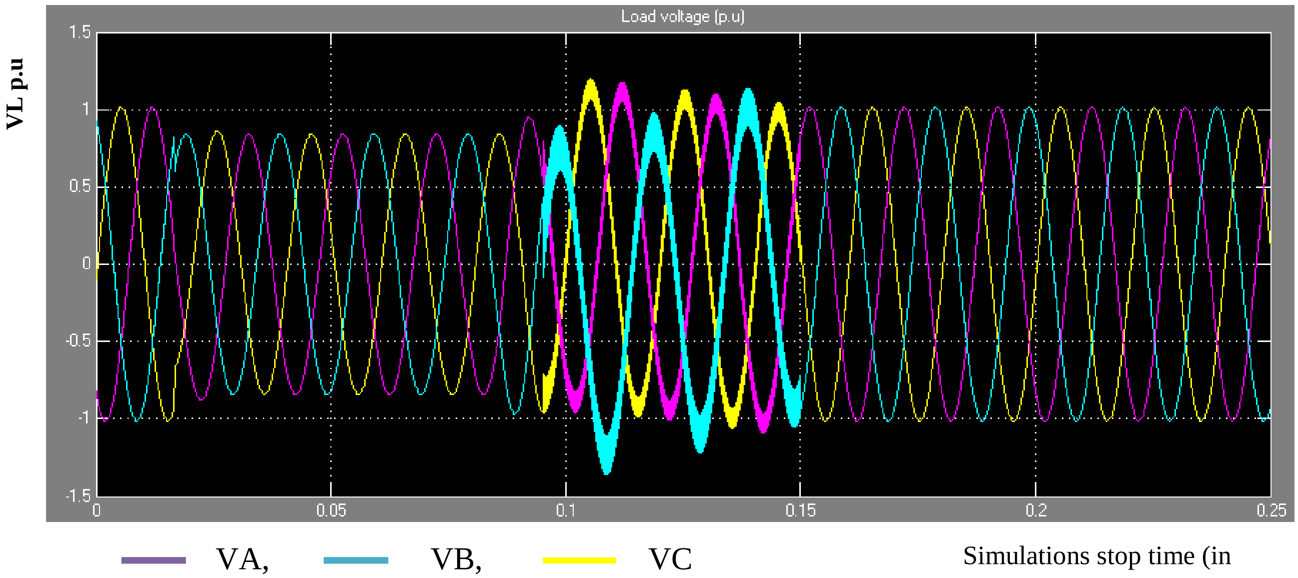

Figure 4.7: Injected voltages [VinjA, VinjB and VinjC] during swell.

In figure 4.8 below shows that the wave of positive sequence during phase to ground fault. The sequence wave was simulated with a three phase fault of starting from 0.0667s to 0.15s and the phase voltage is sag/dip up to (0.304p.u) of its nominal value.

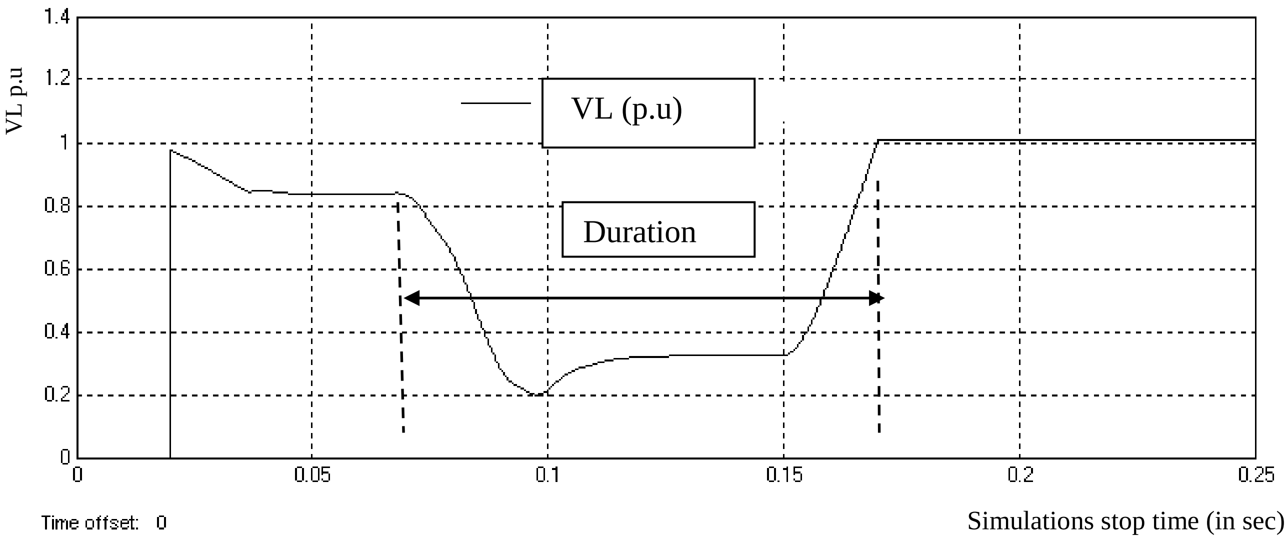

Figure 4.8: Load voltages during a fault (from 0.0667s and to 0.15s) in p.u.

When stored power is delivered from UCAP via DC-DC convertor and DVR device, the compensated output load voltage after mitigation is shown in figure 4.9 below.

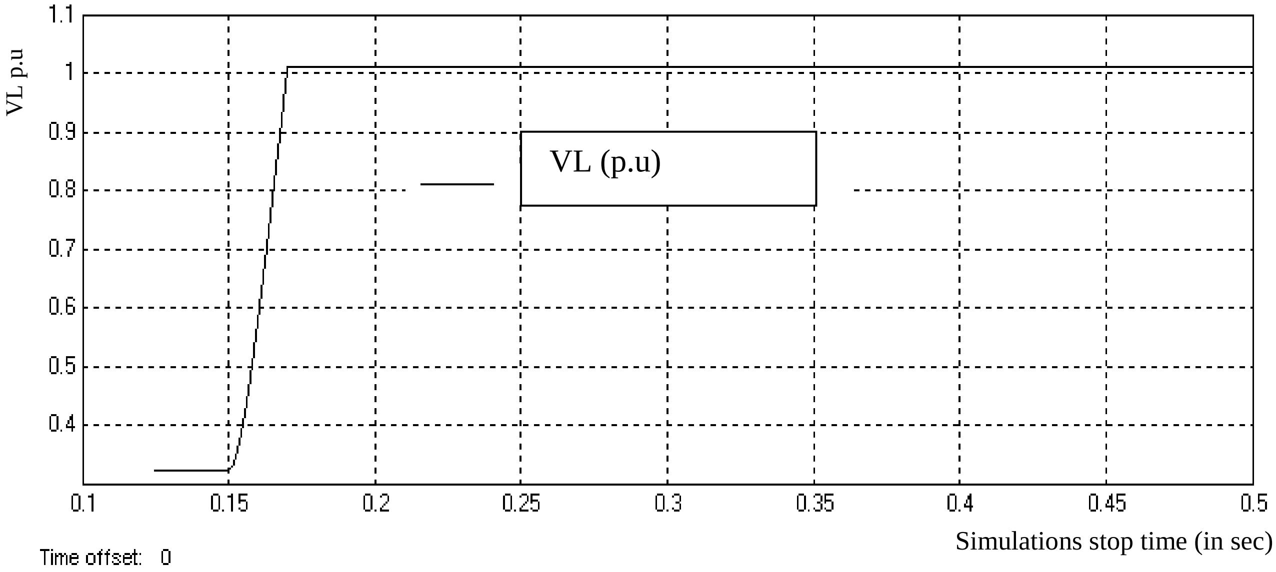

Figure 4.9: Compensated voltage

4.2 Simulation model of UCAP with DC-DC converter

The simulink model of UCAP with DC-DC converter is shown in Figure 4.10 below. There are 81 UCAPs cell connected in series to give 216.8V, which acts as input to the output for preventing the operation at the no-load condition and is connected to the dc-link of the DVR. To simplify simulink model the UCAP cell connected in series are grouped into four places. Each of the groups of UCAP cell has 54.2V. As illustrated in section 3.3.1 to 3.3.3 it's necessary to understand the requirement parameter to size and model the ultra capacitor. Here the considered parameters are energy (J), load power (KW), initial working voltage, discharge time from initial voltage to minimum voltage, total capacitance and discharge current. Actually the voltage of ultra capacitor per cell is small [22] (less than 3V), since it's connected in series to increase the voltage value for high voltage load and it's connected in parallel to increase the requirement current. The charge and discharge time of ultra capacitor is between 0.3second to 30second (Appendix A1).

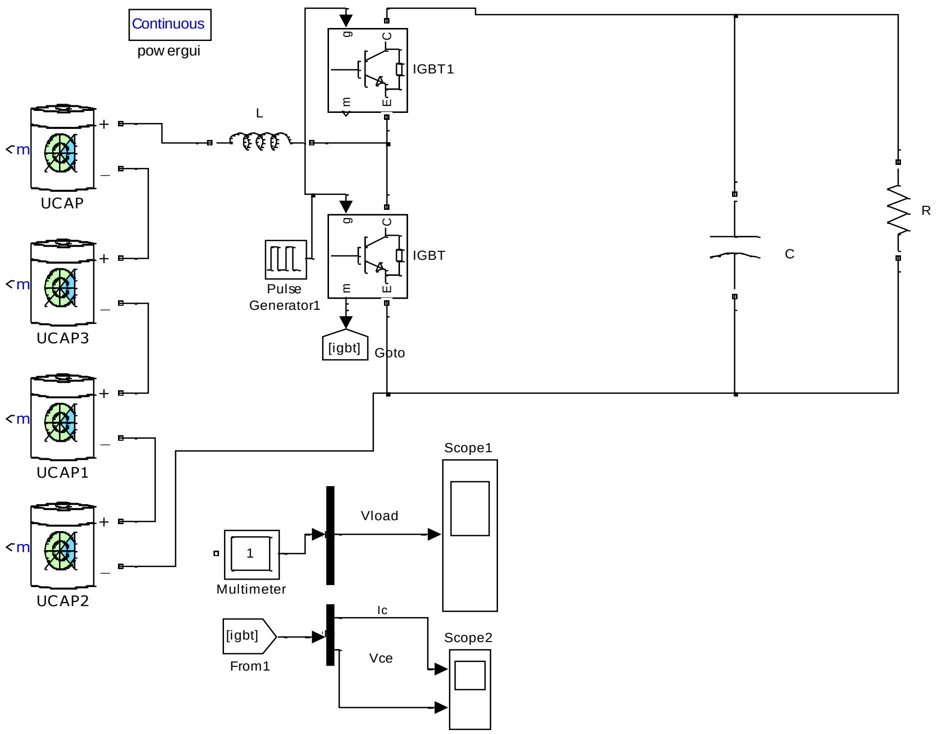

Figure 4.10: Model of UCAP with bidirectional DC-DC converter

Figure 4.11 below shows the input simulation result of UCAP with bidirectional DC-DC converter. For simulation verification 81 cell of ultra capacitor is connected in series (2.7V each per cell) and the combination of each cell becomes 216.8 V.

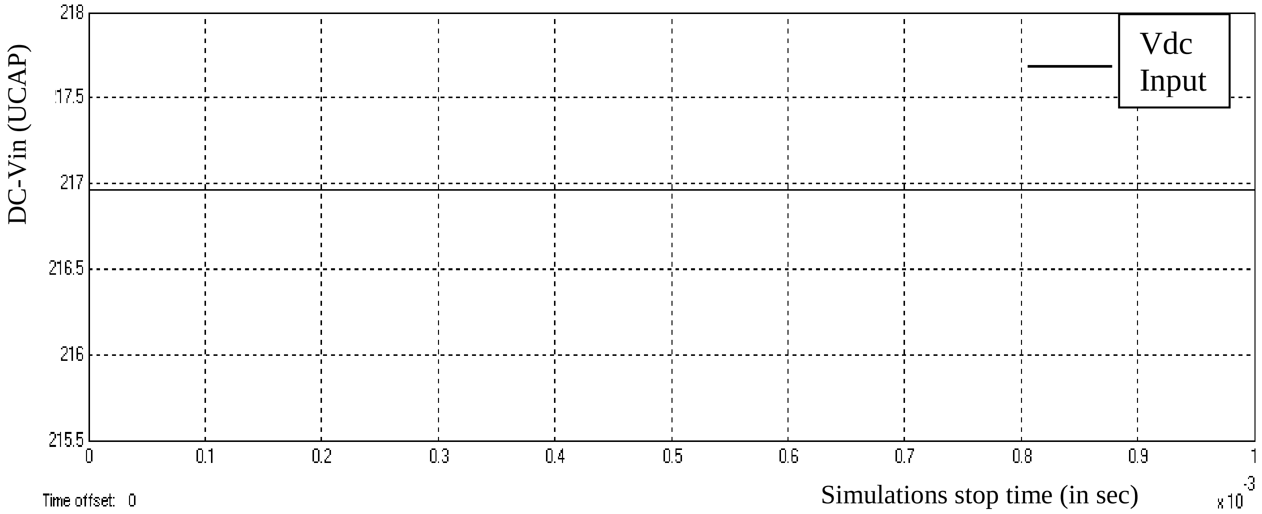

Figure 4.11: input voltage of UCAP

Figure 4.12 below shows the output simulation result of UCAP with bidirectional DC-DC converter. For simulation verification DC-DC boost convertor is supplied from input voltage of UCAP (216.8V) and with duty cycle at 0.277. The DC-DC convertor output voltage simulation is shown in figure 4.12 below cell of ultra capacitor is connected in series (2.7V each) and the combination of each cell becomes 216.8 V.

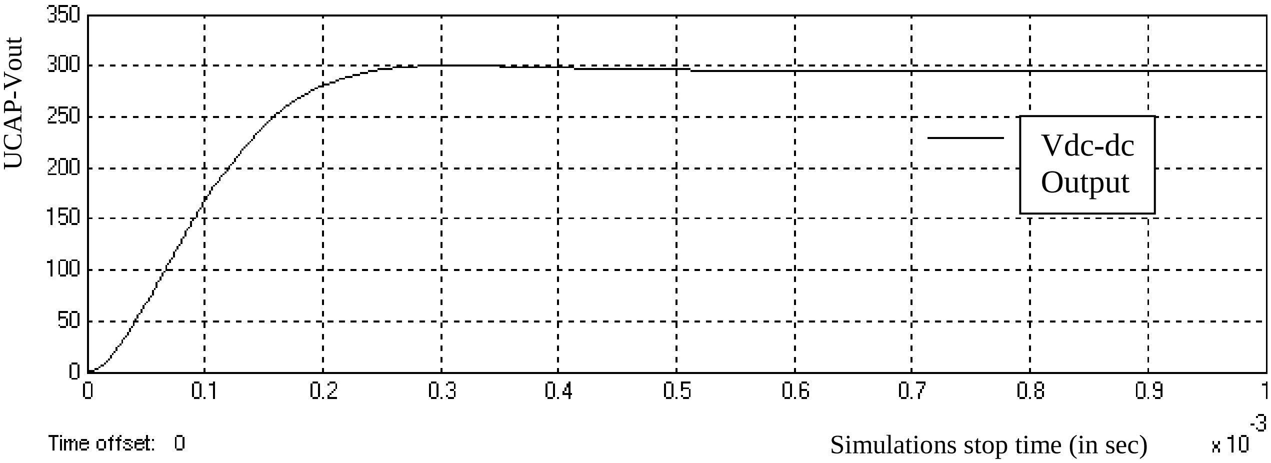

Figure 4.12: Output Voltages of DC-DC converter

4.3 Simulation model of PI controller

The matlab/simulink block diagram of PI controller is shown in figure 4.13.This model shows a voltage-controlled oscillator with feedback control to regulate the output voltage. The oscillation frequency is controlled by the reverse bias voltage applied to the varactor diode (Appendix. E).

Assume that the set point voltage is 1 p.u and when the controller is not triggered the voltage linearly decreases 0.69p.u per millisecond; when the controller is triggered, the system gains 1.125p.u per millisecond. When the controller is not triggered, the system starting point is at the set point voltage with the controller in the OFF mode.

The upper value of the dead band (DB = 12.5%) is 1.125p.u, while the lower value (DB = -69%) is 0.31p.u. This curve (figure 4.8) starts at 1 p.u (SP) and declines at a rate of 0.69p.u/millisecond until the voltage equals 0.31p.u (SP – DB). At 0.31p.u, the controller turns ON and starts flowing the current at a rate of 0.69 p.u/msec until the voltage reaches 1.125p.u (SP + DB), at which point, the controller turns off the flowing current. The process variable (voltage sensor) starts to minimize again at the rate of 0.69p.u/msec until the voltage reaches SP – DB, where the cycle is repeated.

So, the time required to reach SP – DB (0.31p.u) at t1 = 0 and V (t1) = 1p.u is:

V1 (t) = - 0.69p.u (t- t1) + V (t1)

0.31 p.u = - 0.691p.u (t- 0) + 1p.u

t = 1msec

At 1msec, the controller will turn ON. So, knowing that V2 (t) is equal to 0.31p.u at t = 1msec, we need to find the time at t2. V (t 2) is equal to 1.125p.u, because that is the time when the controller will turn OFF again; therefore:

V2 (t) = 0.2(t - t2) + V (t2)

0.31 = 1.125p.u/msec (1msec – t2) + 1.125

t2 = 1.72msec

So, the voltage value will be 1.125 p.u when t = 1.72msec. Thus, the time from the moment the controller turns ON at SP – DB (0.31 p.u) to the moment the controller turns OFF at SP + DB (1.125 p.u) is 1msec. This is the time at 1.125p.u minus the time it took to get to 0.31p.u (1.72msec – 1m sec = 0.72m sec).

To complete the calculation of the oscillation cycle period, we must find the amount of time required for the voltage to minimize to the set point value again. This is equal to 0.72msec of the time it takes for the voltage to go from 1.125p.u to 0.31p.u. Therefore, the frequency of oscillation will be 2.72msec.

The proportional gain relationship between the error and the control variable depends on the width of the band upon which the controller is acting. The voltage control system should have a voltage response that spans from 0.125p.u to 1.125p.u (Vswell), equaling a range of 1p.u (1.125p.u – 0.125p.u). However, if the controller only needs to exert control from 0.31p.u (1p.u-Vsag) to 1.125p.u with the set point at 1p.u, it will only be controlling a range of 0.815p.u (1.125p.u – 0.31p.u) over the total range of 1p.u. Therefore, the proportional band of the controller is 0.815p.u over the 1p.u range and average magnitude of voltage is shown in figure 4.17 below. Accordingly, the proportional band (PB) of control as a percentage of the full process variable range is represented as:

$$PB = \frac{Vlmax - Vlmin}{Vlmax\ range - Vlmin\ range} = \frac{(1.125 - 0.31)p.u}{(1.125 - 0.125)p.u} = 81.5\%$$

$$Gain\ (KP) = \frac{(100 - 0)\%}{81.5\%} = 1.2269$$

$$KI = \frac{\%\ change\ in\ (\frac{dCV}{dt})}{\%error\ over\ full\ range} = \frac{\left(\frac{dCVmax}{dt} - \frac{dCVmin}{dt}\right)}{\frac{(Vlmax - Vlmin)}{Vlmax\ range - Vlmin\ range}} = \frac{(112.5\% - 31\%)}{\frac{(1.125 - 0.31)p.u}{(1.125 - 0.125)p.u}} = 1.76/msec$$

The inverse of the gain term KI is referred to as the integral time (TI), or reset time

T = 1/KI = 0.00056sec

So the output load voltage via transfer function is modeled as shown in figure 4.16 below.

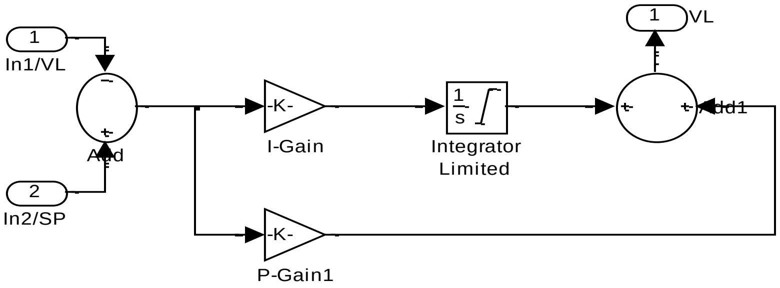

Figure 4.13: Proportional and Integral models

In figure 4.14 the load voltage is entered via ‘In 1’ port as input. Then simulink-PS converter is converts the unit less simulink input signal to physical signal.

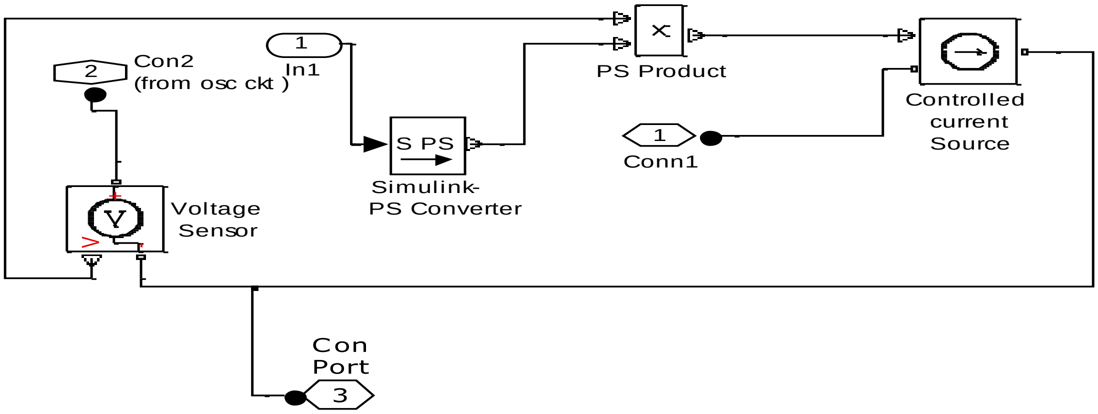

Figure 4.14: Simulink model of control variable

In figure 4.15 PS- simulink converters converts the input physical signal to a unit less simulink output signal. Then the output signal is results as output load voltage via transfer function (figure 4.16).

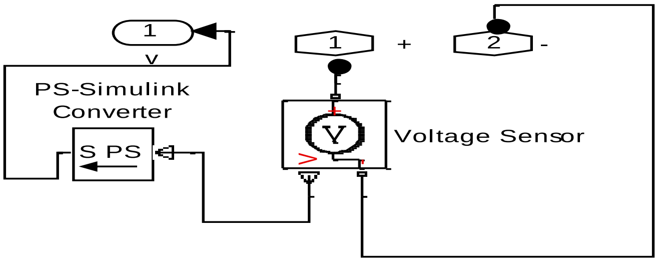

Figure 4.15: model of voltage sensor

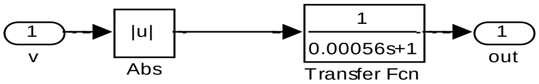

Figure 4.16 Output load voltage via transfer function.

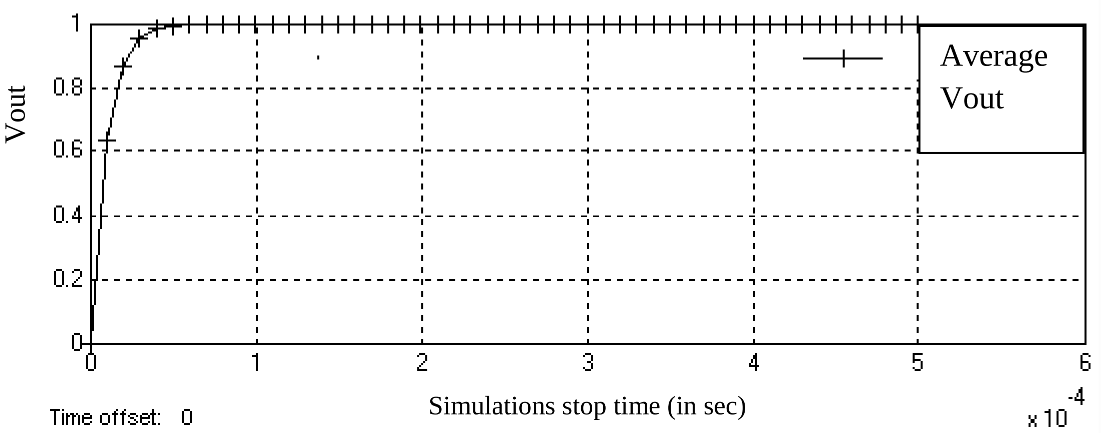

Figure 4.17: Average magnitude of voltage.

5. CONCLUSION AND RECOMMENDATION

5.1 Conclusions

In this paper, the proposed model is equipped with DVR as a suitable FACTS device and the concept of integrating UCAP-based rechargeable energy storage to a power distribution system to improve the power quality of the distribution system is presented. Thus, based on the applied methodology and results obtained, the following conclusions are drawn:

- UCAP integration through a bidirectional dc–dc converter at the dc-link of the power convertor is proposed. The design and modeling of bidirectional DC-DC converter were discussed as UCAP cannot be directly connected to the dc-link of the DVR.
- The UCAP plays an important role; since they can provide very high power in a short duration of time and to explore the feasibility and stability of the energy storage system for improving the electric power quality.
- The control strategy of the series inverter (DVR) is based on in phase compensation and the control strategy of the UCAP-DVR integration is based on PI controller method.
- The DVR handles both balanced and unbalanced situations without any difficulties and injects the appropriate voltage component to correct rapidly any irregularity in the supply voltage to keep the load voltage balanced and constant at the nominal value.
- Designs of major components in the power stage of the bidirectional dc–dc converter are discussed. Average current mode control is used to regulate the output voltage of the dc–dc converter due to its inherently stable characteristic.
- A higher level integrated controller that takes decisions based on the system parameters provides inputs to the inverters and dc–dc converter controllers to carry out their control actions.
- In DVR, filters convert the inverted PWM waveform into a sinusoidal waveform, by eliminating the unwanted harmonic components generated by the VSI action at inductance and equivalent capacitance of 3.67mH and 125μF respectively.

- The sag and swell voltage is presented at 30.4% and 112.5% respectively without integration of UCAP-DVR with three phase fault resistance equal to 0.073 Ω and the load voltage is mitigated with integration of UCAP-DVR at DVR voltage of 70.5 %.
- The simulation of the integrated UCAP-DVR system which consists of the UCAP, bidirectional dc–dc converter and the series inverters is carried out using MATLAB. The load voltage sin wave is simulated with a three phase fault of starting from 0.0667s to 0.15s and the phase to ground voltage is sag/dip up to 30.4 % (0.304p.u) of its nominal value.
- The load voltage sin wave is simulated during three phase injection voltage starting from 0.0667s to 0.15s. Simulation result shows that the proposed UCAP - DVR provide compensation in efficient and deep manner.

5.2 Recommendation

- It is known that in Ethiopia somewhat there is the reliability of power distribution. But now days due to non linear device, there is sensitive load at customer or user side. So the customer/commercial does not worry only the reliability of the power distribution, but also they worry about the power quality.
- There is an impact of power quality problem at EEU side, such as equipment tripping, reduce of monthly payment, damaging of equipment, the wastage of time and money during maintenance.
- And the impact at the user side is wastage of production, equipment tripping, system crash, to pay expenditure for maintenance and etc. Therefore, it is recommended to use the custom power device to mitigate the power quality problem.
- The proposed system is may be initially cost but if we compare with the disadvantage of the power quality problem, it’s the better solution.

5.3 Future work

The future scope of the calculated and simulated results can be done experimentally and practically. And also there is the limitation of integration of UCAP-DVR which is not overcome for permanent fault. For future work it will include to mitigate the voltage for permanent fault by integrating DVR with high energy storage device such as SMESS.

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[24] Hawassa Substation

APPENDIX

Appendix A1. A comparison of conventional storage technology, www.maxwell.com

Available performance	**Lead Acid battery**	**Conventional Capacitor**	**Ultra Capacitor**
Charge time	1 to 5 hrs	10^{-3} to 10^{-6} s	0.3 to 30 sec
Discharge time	0.3 to 5 hrs	10^{-3} to 10^{-6} s	0.3 to 30 sec
Energy (Wh/Kg)	10 to 100	< 0.1	1 to 10
Power density	< 1000	< 100000	<10000
Cycle Life	< 1000	> 500000	>500000
Charge/discharge Efficiency	0.7 – 0.85	> 0.95	0.85 – 0.98

Appendix A2. Maxwell production Cell Maximum Leakage Current, www.maxwell.com

Product	**Nominal capacitance (F)**	**Leakage current Maximum (mA)**
BCAP25	25	0.045
BCAP50	50	0.075
BCAP310	310	0.45
BCAP350	350	0.3
BCAP800	800	1.5
BCAP1200	1200	2.7
BCAP1500	1500	3
BCAP2000	2000	4.2
BCAP3000	3000	5.2
BCAP3400	3400	15

Appendix B. Hawassa Substation Circuit breaker specification

NO	**ITEM NAME**	**Transformer-1**	**Transformer-2**	**Transformer-3**	**Yirgalem Outgoing**
1	Type	HLD145/1250C	HPL145/25A1	GL313F1	LTB17001/B
2	Serial Number	2257352	7737286	5312-10-2010078/1	8660571
3	Voltage (kV)	145	145	170	170
4	Normal Current (A)	1250A	2500A	3150A	3150A
5	Short Circuit Breaking Current (kA)	2527.5A	40KA	10KA	40KA
6	Making Current	62.5KA	100KA	-	100KA
7	Rated Insulation Level (kV)	650/275	650/275KV	-	750-325
8	Make	Sweden	Sweden	Germany	Sweden
9	Year of Manufacture	1979	1988	2005	2003

Appendix C1. Load data from Hawassa substation

NO	**ITEM NAME**	**Yirgalem**	**Feeder 1**	**Feeder 2**	**Feeder 3**	**Feeder 4**	**Feeder 5**	**Feeder 6**
1	Voltage level	132KV	15KV	15KV	15KV	15KV	15KV	15KV
2	CT ratio	300-600/1A	200-400/5A	50-100/5A	50-100/5A	200-400/5A	400-800/1A	400-800/1A
3	Load (A) max	185	232A	61.58	66	240A	280A	167A
4	Active Power PLoad (MW)	33.8	4.9	1.28	1.4	4.34	6.4	3.18
5	Reactive Power QLoad (Mvar)	25.35	3.67	0.96	1.05	3.25	4.8	2.38
6	Status (in service or not)	In Service	In Service	In Service	In Service	In Service	In Service	In Service

Appendix C2. Load data from Hawassa substation

NO	ITEM NAME	Feeder 7	Feeder 8	Feeder 9	Feeder 10	Feeder 11	Feeder 12	Feeder 13
1	Voltage level	15KV	15KV	33KV	33KV	33KV	15KV	15KV
2	CT ratio	400-800/5A	400-800/1A	75-150/1A	75-150/1A	75-150/1A	400-800/1A	400-800/1A
3	Load (A) max	77	110	9	18	52	96	167
4	Active Power P load (MW)	1.6	2.6	1.6	0.9	0.33	2.23	3.44
5	Reactive Power Q load (Mvar)	1.2	1.95	1.2	0.675	0.247	1.67	2.6
6	Status (in service or not)	In Service	In Service	In Service	In Service	In Service	In Service	In Service

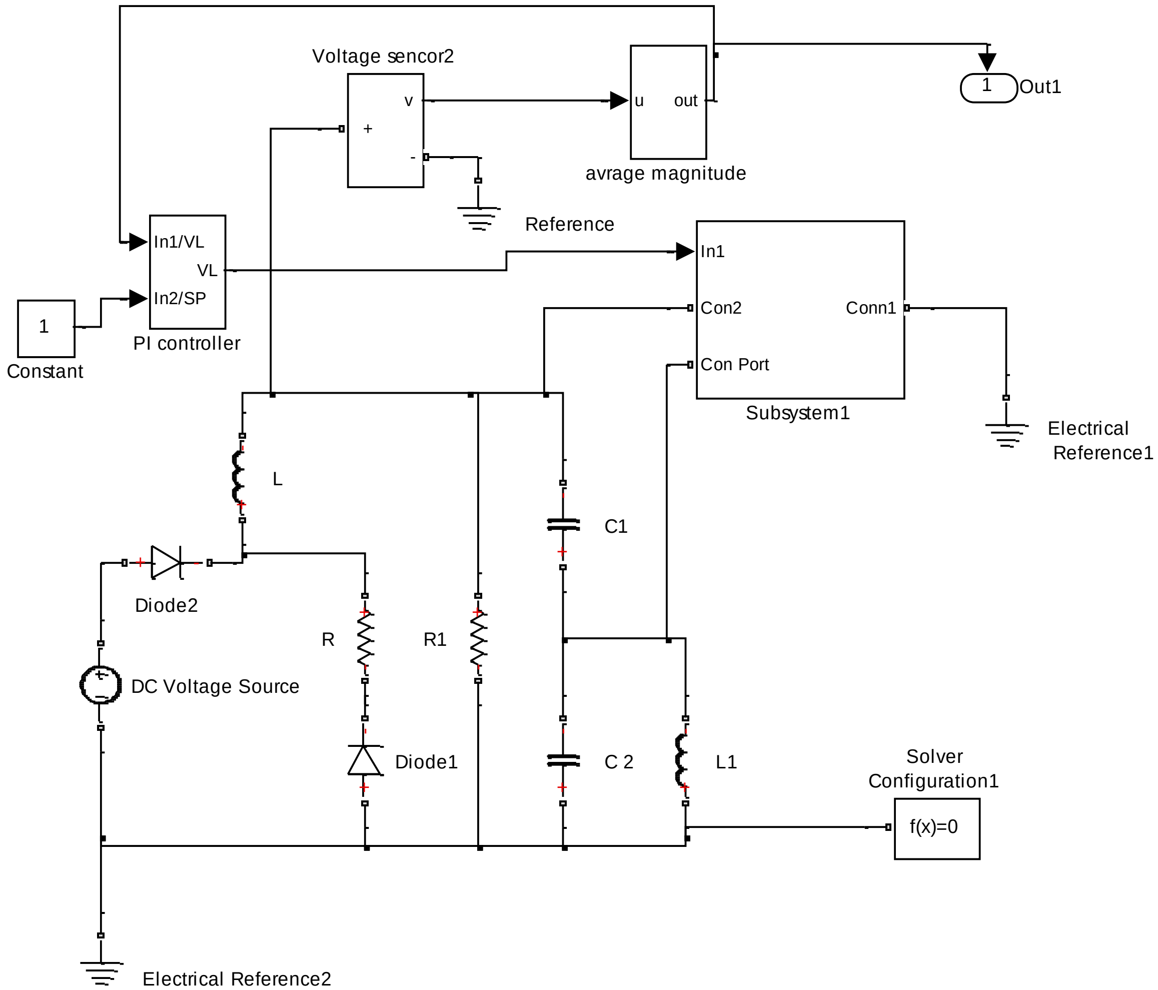
Appendix D1.Total number of frequency interruptions and total duration of interruption data per month (July, 2016).

Line (L)	Pef /month	Psc/month	Tef/month	Tsc/month	Sol/month	Oper/month	Total duration of interruption(Hr)
1	1- times	4 - times	2 - times	12 - times	No	9 - times	47
3	No	No	No	No	No	1 - times	2
4	4- times	6 - times	2 - times	4 - times	No	12 - times	36
5	4- times	4 - times	5 - times	12 - times	No	7 - times	16
6	6- times	3 - times	6 - times	9 - times	No	10 - times	25
7	No	3 - times	7 - times	14 - times	No	9 - times	30
8	No	2 - times	No	4 - times	No	1 - times	15
9	No	No	No	No	No	9 - times	12
10	13 - times	17 - times	4 - times	10 - times	No	11- times	21
11	No	2 - times	No	No	No	3 - times	4
12	6- times	7 - times	7 - times	10 - times	No	13 - times	9
13	5- times	4 - times	2 - times	11 - times	No	7 - times	27
14	1- times	1 - times	No	No	No	3 - times	1.55

Appendix D2.Total number of frequency interruptions and total duration of interruption data per month (September, 2016).

Line (L)	Pef /month	Psc/month	Tef/month	Tsc/month	Sol/month	Oper/month	Total duration of interruption(Hr)
1	2 - times	3 - times	2 - times	10 - times	No	5- times	20.3
3	7- times	No	No	5 - times	No	1 - times	3.5
4	4- times	7 - times	2 - times	4 - times	No	9 - times	11
5	3- times	5 - times	5 - times	13 - times	No	7 - times	16
6	6- times	3 - times	6 - times	9 - times	No	10 - times	19
7	6- times	3 - times	11 - times	12 - times	No	9 - times	28.4
8	No	2 - times	No	No	4 - times	1 - times	17.35
9	No	1 - times	No	6 - times	No	9 - times	14
10	13- times	17 - times	4 - times	10 - times	No	11- times	18
11	No	2 - times	No	No	No	3 - times	11
12	6 - times	7 - times	7 - times	10 - times	No	13 - times	15
13	5- times	4 - times	2 - times	11 - times	No	7 - times	21
14	10times	1 - times	No	9 - times	No	3 - times	13.35

Appendix E. proportional and integral with oscillator frequency controlled circuit



Appendix F. Back-boost transformer character

	Boost- increase voltage										**Buck-decrease voltage**					
Load (V)	208	208	208	230	240	240	416	416	416	416	208	208	240	240	416	416
Line (V)	166	173	187	208	216	228	374	377	395	397	230	249	252	264	437	457
Load amps (A)	67	83	144	165	74	158	75	83	158	166	183	99	175	92	173	92
KVA	24	30	52	65.8	31	66	54	60	114	120	66	36	72.8	38.1	124.8	66
Line fuse	110	150	225	250	110	250	110	125	250	250	225	110	225	110	225	110